High Power, Broadband, Linear, Solid State Amplifier

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13. ABSTRACT (*Maximum 200 words*) AlGaN/GaN MODFET's grown by MBE and OMVPE with less than 25 μm gate lengths, yield up to 50 and 100 GHz for f_t and f_{max} respectively. A substantial effort on circuits for combining power, including both direct power combining and traveling wave combining has been started, along with experimental studies of large pheriphery devices. A new analytical model for the effect of dislocations on electron mobility has been made, and electron transport in III-nitrides has been studied using the Monte Carlo method.Epitaxial growth on SiC and sapphire is being carried out by both MBE and OMVPE, and studied by high resolution STEM. Bulk crystallites 250 μm in diameter, have been grown and will be used as seeds for growth of larger boules.

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I. Overview

Overview of Cornell MURI Program on High Power, Broadband, Linear, Solid State Amplifier - L.F. Eastman

This is the first annual report on a project to achieve a linear amplifier capable of an output power of 100 W with over 60% efficiency, and over a multi-octave frequency range covering X-band. Field effect transistors are being employed, including AlGaN/GaN MODFET's and GaN vertical current flow static induction transistor (SIT's). These devices are capable of an order of magnitude more operating voltage, and an or der of magnitude more power density when SiC substrates are used, than their GaAs equivalents. Because of the higher voltage, a proportionately higher normalized optimum load impedance is possible, leading to larger periphery values. By combining a set of four or more of the resulting power cells in either ordinary power combiners, or traveling wave power combiners, the output power of 100 W at high efficiency is possible.

Initial MODFET devices, made from MBE and OMVPE material, with sufficient frequency response ($f_t > 30$ GHz, $f_t > 55$ GHz), have been achieved after ohmic contact optimization. SIT devices have been simulated, and all the process for fabricating these devices have been developed. Power amplifier topologies, using hybrid circuits, have been developed and will be simulated using measured power transistor parameters. A standard matrix of 25 different power transistor, ranging from 50 μm to 3,200 μm periphery, will be processed on both sapphire and SiC substrates, and measured. The optimum normalized load resistance for these power transistors designed to be 100 Ωmm. Simulation of heat flow and thermal resistance has been completed on the MODFET's on SiC substrates, yielding 10...20 °mm/W, depending on the pitch distance between parallel MODFET's. This is an order of magnitude lower than for sapphire substrates.

Theoretical studies of the materials structure, the design of the deep submicron MODFET's, the effect of dislocations on mobility, and on high-field electron transport using the Monte Carlo method have been made. SiC substrates have been supplied by subcontractor Northtrop Grumman. These have been mostly N^+ type to date, but more V-doped semi-insulating substrates will become available. Bulk GaN crystal growth using movel techniques has yielded small (250 μm) single crystal, and large crystals will now be made using big seeds. Both MBE and OMVPE growth have progressed with reasonable growth rates, and with calibrated Si doping. The OMVPE equipment, yielding low net donors (low $10^{16}/cm^3$), is capable of multi-wafer growth. Finally, very high-resolution characterization has begun, following the development of sample preparation using a high voltage UHV STEM.

II. Discrete GaN Transistors

A. Summary - L. F. Eastman

HFET research has yielded excellent ohmic contact contact resistance (0.25...0.60 Ωmm) and good frequency response ($f_t > 30$ GHz and $f_{max} > 55$ GHz) for small periphery devices. A matrix of power devices ranging from 150 μm to 3,200 μm periphery will be fabricated, on sapphire and SiC substrates, for evaluation for amplifiers. Vertical, S.I.T. type, devices have been

simulated yielding 8 GHz f_t and 80 GHz f_{max} and designs have been made. The necessary process steps have been optimized and initial fabrication is using HVPE material from Lincoln Labs.

B. Discrete Transistors: GaN HFET's - Ken Chu

In the past year progress was made in making ohmic contact to III-V nitride layers and understanding the gate breakdown mechanisms in our layer structures. As a result of improved ohmic contacting, source and drain contact resistances are now insignificant compared to the intrinsic electron channel resistance. Also, Schottky gate breakdown studies has led to new layer structure designs with thicker AlGaN barrier thickness and lower electron sheet density, both of which are believed to help increase the gate-drain breakdown voltage.

1. Ohmic contact development

Low resistance ohmic contacts with relaxed annealing conditions were developed on AlGaN/GaN HFET layers. Different ohmic metallization schemes were deposited on an MBE-grown HFET wafer and annealed at 800°C, while their contact resistances were monitored as a function of annealing time. 800°C was chosen instead of the usual annealing temperature of 900°C to minimize any surface damage induced by annealing. After annealing, Ti/Al/Ti/Au (200 Å/ 1000 Å/ 450 Å/ 550 Å) gave a contact resistance of 0.60 Ω mm with a specific contact resistance of 3.44 x 10^{-6} Ω cm^2, while Pd/Al/Ti/Au (200 Å/ 1000 Å/ 450 Å/ 550 Å) demonstrated 0.25 Ωmm and 5.95×10^{-7} Ωcm^2. However, adhesion of the Pd-based contact to the nitride surface has to be improved. Also, it was noteworthy that the sheet resistance of the material stayed constant at 1030 Ω per square through the 120 s of 800°C annealing, suggesting that the surface damage (nitrogen desorption) induced by the anneal was minimal.

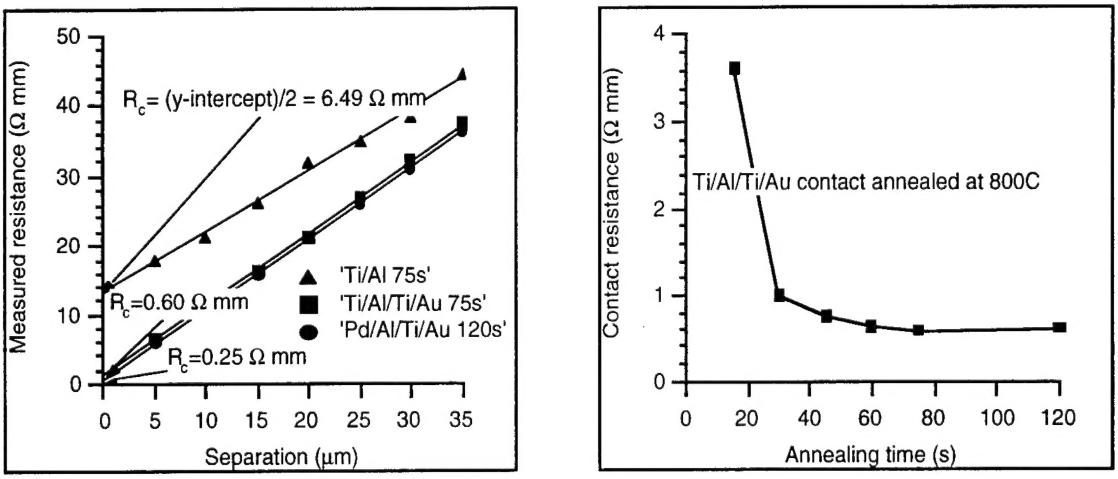

Figure 1. TLM measurement of ohmic contact resistance on AlGaN/GaN HFET layers

2. HFET fabrication using improved ohmic contacts

The ohmic contacting scheme with Ti/Al/Ti/Au was then utilized to fabricate AlGaN/GaN HFET's. The structure included (from bottom to top) a sapphire substrate, 0.1 μm of AlN nucleation layer,

1.5 μm of undoped GaN, 20 Å of undoped AlGaN spacer, 20Å of Si-doped AlGaN layer (N_d = $7x10^{19}$ cm^{-3}) and 110 Å of undoped AlGaN barrier. The Al mole fraction used in all the AlGaN layers was 0.3. Hall measurements showed a mobility of 405 cm^2/V s and an electron sheet density of 1.67 x 10^{13} $/cm^2$.

The transistor fabrication process included mesa isolation, ohmic contact formation, connection pad deposition and gate metallization. After annealing the ohmic metal at 800°C for 60 s, a low contact resistance of 0.24 to 0.4 Ω mm was measured with TLM patterns. This variation of contact resistance was attributed mainly to non-uniformity of the wafer, as the wafer was not rotated during growth. T-shaped gates were defined by electron beam lithography and formed by evaporating Pt/Au (400Å/ 2600Å) or Ni/Au (200Å/ 2800Å). The Ni metallization was found to adhere better to the nitride surface and gave a higher yield in the gate lift-off process, particularly for short gate length devices. Using SEM, the gate lengths were estimated to be varying from 0.15 to 0.28 μm, a direct result from variation of the exposure dose. Nominal gate-drain spacings were 0.75 and 1 μm.

Shown in Figure 2(a) is the DC current-voltage characteristics of the fabricated transistors. The maximum drain current was above 1 A/mm, a result of the high electron sheet density of the material. (Measurement was stopped at 1 A/mm due to the current compliance of the measurement system.) Maximum DC transconductance was 182 mS/mm. Linear and steep current-voltage characteristics at low drain biases signify the excellent quality of the ohmic contacts. Total drain-source resistance was measured to be 2.6 Ω mm, of which only 0.6 Ω mm (or 23%) came from the source and drain contact resistances.

As seen in Figure 2(a), there was a non-zero output conductance, particularly for lower current levels. This was attributed to short-channel effects created by the short gate length and the absence of a backside barrier to the conduction channel. At higher current levels the output conductance was reduced and even became negative. This was due to the additional effect of carrier mobility lowering with increasing temperature.

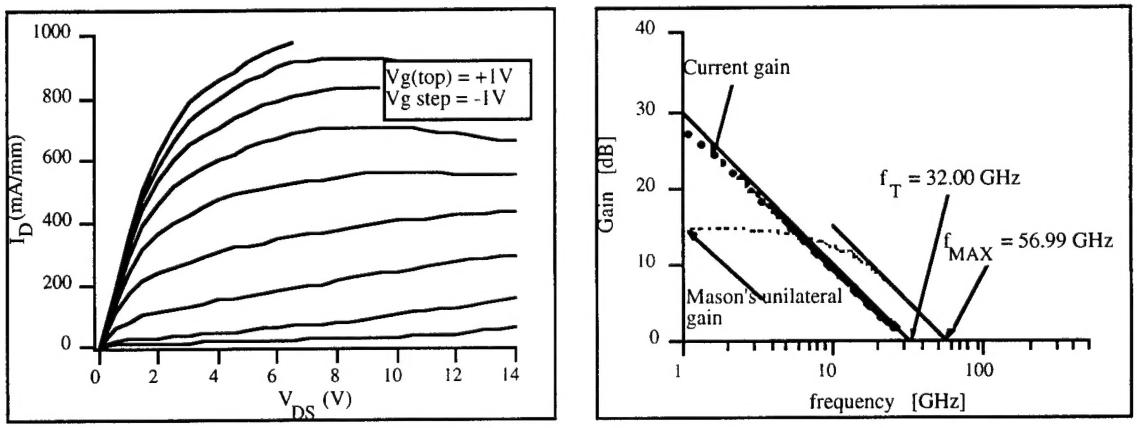

Figure 2. (a) DC characteristics of the AlGaN/GaN MODFET's showing drain current over 1 A/mm, and (b) RF performance of a 75 μm periphery device

Despite a thin barrier, good ohmic contacts and high electron sheet density, the measured static transconductance (g_m) was only 182 mS/mm, 13% lower than the result obtained in another layer structure with the same AlGaN barrier thickness [1]. One possible reason is electrons trapped in the AlGaN barrier (in traps or at the conduction band minimum of the donor layer) which would then have a screening effect on the gate potential, reducing the effectiveness of charge modulation by the gate.

Figure 2(b) gives the RF performance of a 75 μm periphery device. An f_T of 32.0 GHz and an f_{max} of 57.0 GHz were achieved. A similar device with a 100 μm periphery demonstrated an f_t of 35.9 GHz and an f_{max} of 54.8 GHz. SEM studies showed a gate length of 0.15 μm for these devices. Although the ohmic contact was greatly improved compared to devices in reference [2], the RF performance was not as good. This could be attributed to a different layer structure and longer gate lengths utilized.

An estimate of the electron saturation velocity (v_{sat}) in our structure can be obtained from the RF data as follows. For a field effect transistor, total time delay for electron transit (τ_{total}) can be given by

$$\tau_{total} = \frac{1}{2\pi f_T} = \tau_{RC} + \tau_g + \tau_{gd} \tag{1}$$

where τ_{RC} is the RC time contant for charging the gate capacitances, τ_g is the transit time of electrons under the gate and τ_{gd} is the delay time for electrons to traverse the gate-drain separation. They are in turn given by

$$\tau_{RC} = \left(R_g + R_s\right)\left(C_{gs} + C_{gd} + C_{gpad}\right) \tag{2}$$

$$\tau_g = \frac{L_{g,eff}}{v_{sat}} \tag{3}$$

$$\tau_{gd} = \frac{L_{gd} + L_{transfer}}{2v_{sat}} \tag{4}$$

where R_g is the gate access resistance, R_s is the source resistance, and C_{gs}, C_{gd} and C_{gpad} are gate-source, gate-drain and gate pad capacitances respectively. $L_{g,eff}$ is the effective gate length which includes the fringing field effect. L_{gd} is the physical gate-drain separation and $L_{transfer}$ is the drain ohmic contact transfer length. The factor of 2 in equation (4) comes from the fact that here an induced current is passing through a region with a relatively constant field [3], as is the case of bipolar transistors where the collector depletion transit delay takes on a similar expression.

Substituting the appropriate values from various DC measurements and RF parameter extraction, we have an estimate of the electron saturation velocity in our structure:

$$v_{sat} = 1.3 \times 10^7 \text{ cm/s}$$

which is about 60% of the theoretical value obained from Monte Carlo calculations [4]. (This simple estimation is optimistic because we are assuming that the depletion region from the gate reaches the drain contact.) As material quality and processing techniques continue to improve, this saturation velocity value is expected to increase towards the theoretical maximum.

3. Gate-drain breakdown studies

For these transistors to be useful as power devices, they must have a high maximum drain current together with a high breakdown voltage at pinch-off. Maximum drain current was high and above 1 A/mm, but these devices showed only a modest gate-drain breakdown voltage of 30 to 35 V, much less than some of the best results achieved in GaN based field effect transistors (> 200 V for large gate-drain spacing). This prompted us to study the exact mechanism for breakdown in these devices.

From our measurements we observed a relatively high gate leakage current under pinch-off conditions. Since the electron sheet density in our layer structure was very high (n = 1.67 x 10^{13} cm^{-2}), there would be a very high electric field underneath the gate in pinch-off conditions (> 4 MV/cm), giving rise to increased tunneling current. Any additional field that comes from drain bias and field crowding effects for very short gates further worsen the situation. To confirm this is indeed the reason for our low breakdown voltages, gated-TLM structures were constructed on the same wafer. 2-terminal gate-drain reverse breakdown characteristics were compared for different ohmic-Schottky separations and for different gate-lengths. Figure 3 shows the measured result. We can see that the breakdown voltage variation with gate-drain spacing was small as opposed to common observation, suggesting that the major breakdown mechanism occurred close to the gate, possibly tunneling in this case, and was not very sensitive to changes in gate-drain separation. Furthermore, breakdown voltage increases with gate-length, which suggests that field crowding effects near the gate were indeed present in our structure. An average gate-drain breakdown voltage of 22.6 V for 0.15 μm-gates, 33.8 V for 0.3 μm-gates and 51.6 V for 1 μm-gates were obtained. Moreover, the large variation of breakdown voltages for the same gate-length suggests that the breakdown voltage was sensitive to the local material quality.

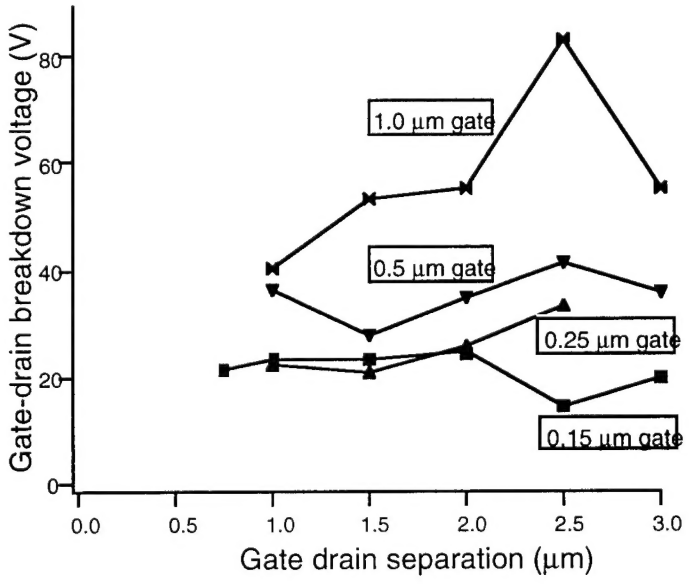

Figure 3. Gate-drain breakdown voltages for different gate-drain separations and different gate lengths

4. Future work

Future work in nitride HFET's include designing new layer structures and developing new device fabrication technology. From the above observations, we conclude in order to achieve high breakdown voltages we need to decrease the electron sheet density to around 1 x 10^{13} cm^{-2} in future layer designs. This will decrease the field strength beneath the gate in pinch-off conditions. Moreover, in the near future we plan to fabricate transistors on highly resistive and semi-insulating SiC. These devices will allow higher power operation due to better heat conductivity of the SiC substrate. On the device fabrication side we will fabricate transistors with a longer gate-periphery to get more power out of a single device and more importantly, to get better impedance matching in our circuits. Multiple gate fingers (>2) will be necessary to reduce the resistive voltage drop along the thin T-shaped gate fingers, so these devices will utilize source air-bridge technology which has already been developed and tested in this group.

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C. Vertical GaN Microwave Transistor - Nils Weimann

1. Introduction

This report covers the research activities on Vertical GaN Power Microwave Transistors at Cornell University in the first year of the MURI on Broadband Microwave Amplifiers. The goal of high efficiency (60%), high power (100 W) solid-state amplifiers operating at X-band can only be achieved using transistor devices on wide bandgap semiconductors (GaN, SiC), enabling the use of high power supply voltages (> 100 V), and taking benefit of the thermal properties of these materials.

The physical and technological aspects of the feasibility of a vertical GaN transistor, also known as Static Induction Transistor (SIT), are discussed in the following sections. The concept of using Static Induction Transistors for high-frequency power amplifiers has been proven by Northrop-Grumman, their SiC SIT-based Digital-Broadcast TV amplifiers operating at about 800 MHz are already being commercialized.

2. Design and simulation of the GaN vertical transistor

Device operation of the SIT is strongly dependent on the device geometry and doping concentration. Due to the lack of an analytical model of drain current as a function of terminal voltages, 2D numerical analysis is performed using the ATLAS simulation software package from Silvaco, Inc. to optimize the SIT geometry.

The source contacts are on top of the device, interdigited with recessed gate fingers. The drain contact is located on the back of the conducting SiC substrate (see Figure 3).

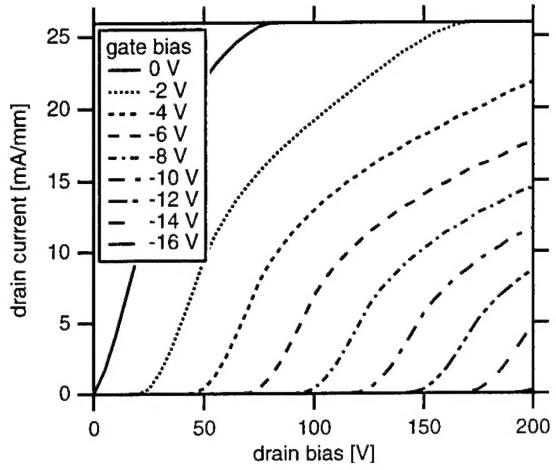

Figure 1: simulated output curve gate voltage 0 (top) to -16 V (bottom)

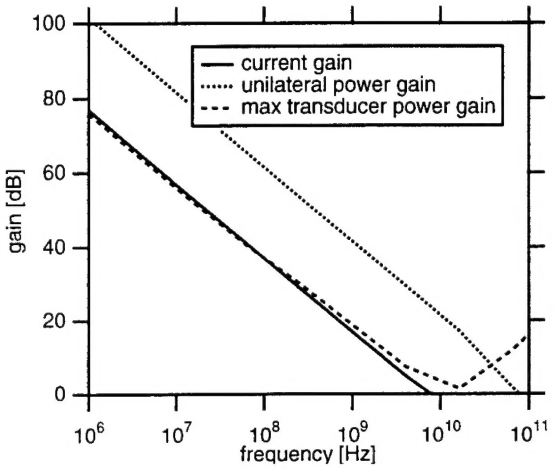

Figure 2: simulated small-signal gain curves, V_D = 100 V, V_G = -8 V

The thickness of the GaN layer is determined by the maximum operating voltage of the device, yielding 3 μm for a maximum field of 1 MV/cm and 300 V operating voltage. The highest field occurs at the edges of the recessed gate contact. Simulation results do not show field strengths greater than 3 MV/cm for pinch-off, with a supply voltage of 200 V at the drain and a gate voltage of -20 V.

The width of the source finger corresponds to twice the individual gate depletion width, and is hence only dependent on the doping concentration. The distance between gate and source is chosen greater than 0.3 μm to avoid breakdown. The length and position of the gate are optimized for maximum drain current and voltage gain. As an example, a structure optimized for a donor density of 10^{15} cm^{-3} is shown in Figure 3.

DC curves are simulated using the following parameters: donor density 10^{15} cm^{-3}, Schottky barrier height 1 eV, low-field mobility 1500 cm^2/Vs, saturation velocity $2.7 \cdot 10^7$ cm/s, using a simple velocity model that approaches saturation monotonically, to prevent numerical instabilities. This is justified by the expected small difference between maximum velocity and saturated velocity from Monte Carlo simulations. The Poisson and carrier continuity equations are solved simultaneously for various bias points. Resulting drain current vs. drain voltage curves are shown in Figure 1. As only one half of the source finger is simulated, the total drain current is obtained by multiplying the scaled drain current by twice the device width times the number of source fingers. The total device periphery is determined by the desired output impedance. The number of source fingers is chosen to minimize phase delays along the gate and source fingers.

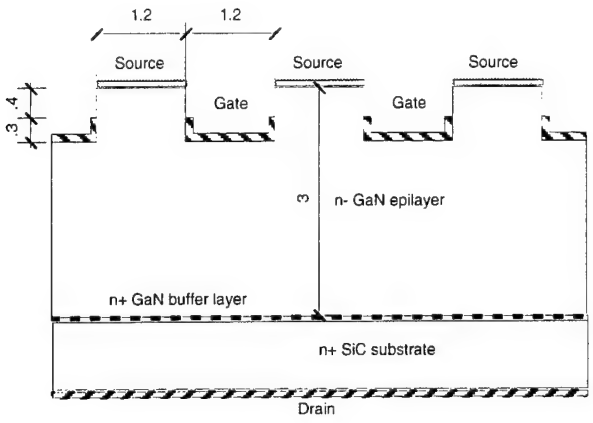

Figure 3: SIT schematic (dimensions in μm)

High-frequency performance of the SIT structure can be evaluated by small-signal AC simulations. A small sinusoidal signal is superimposed on a given DC bias. The admittance matrix for the source, gate and drain contacts is computed from the linearized time dependent semiconductor equations. This simulation includes parasitic contact capacitances, e.g. the gate-source capacitance C_{gs} and the gate-drain feedback capacitance C_{gd}. The admittance matrix is converted to S-parameters using the appropriate device width, then the current and unilateral power gain are computed. Figure 2 shows unity current gain occurring at f_t = 8 GHz, and unity power gain at f_{max} = 80 GHz.

3. Vertical GaN transistor process

The minimum dimension of a SIT for a doping density of 10^{17} cm^{-3} is the source finger width of 0.6 μm. This feature size can be reproduced using the optical UV 10:1 reduction stepper in the Cornell Nanofabrication Facility (CNF). The current process design employs four mask levels.

1. Source pad isolation: the GaN SIT is a normally-on vertical device, the source pad has to be isolated to prevent parasitic current flow. A 0.15 μm thick SiN isolation layer is deposited by Plasma-Enhanced Chemical Vapor Deposition (PECVD) on top of the n^+ GaN cap layer and patterned using Reactive Ion Etching (RIE) etching after a positive lithography step.

2. Source metal: the ohmic source metal is evaporated on a liftoff mask.

3. Gate recess: the gate wells are etched by Electron Cyclotron Resonance (ECR) RIE after a positive lithography step. The whole structure is covered with SiO_2 deposited by PECVD, and planarized using Chemical-Mechanical Polishing (CMP). The oxide is etched back to the height of the sidewall gates.

4. Oxide removal: after a lithography step, the top and the sides of the source fingers are covered with photoresist. The oxide is removed, leaving only the top of the source fingers covered, and the Schottky gate metal is evaporated and lifted.

5. an optional fifth mask step exists for test structures of GaN on sapphire, enabling contact formation on the drain, via a conducting buffer, from the top of the device.

4. Device fabrication status

The optical mask set for the 10:1 stepper is completed. Due to lack of GaN layers grown on SiC substrates, device fabrication is limited currently to test structures based on thick GaN layers (3...5 μm) on sapphire substrates, deposited using HVPE at Lincoln Labs.

Si was implanted in the surface of the GaN layers for ohmic contacts on the undoped GaN. The ECR-RIE etch is calibrated, yielding etch rates up to 1600 Å/min with high aspect ratio. SiO_2 and SiN have been deposited successfully on GaN using PECVD.

5. Summary and outlook

The transport properties of dislocated GaN are readily understood on a macroscopic scale. The electronic and thermal design of SIT structures is performed using 2D numerical simulations, showing the possibility of a SIT device operating at 10 GHz with an output power of up to 100 W into a 50 Ω load. A process for SIT device fabrication based on optical lithography is currently developed.

The next experimental steps will be completion of the GaN SIT test structure on sapphire, and testing of devices. For the modeling of SIT devices, lattice heating effects will be included in the electronic simulations.

Future work will include the evaluation of a ballistic AlGaN source cap on top of the GaN channel material. Monte Carlo simulations show possible ballistic transport on a length of up to 0.2 μm. The SIT process will be extended to air-bridged source and gate terminals to reduce parasitic pad capacitance, and include a fifth mask level to remove the gate metal from the bottom of the gate trenches for reduced gate-drain feedback capacitance.

III. Amplifiers and Heat Sinking

A. Summary - L.F. Eastman

Two hybrid power amplifier circuits have been chosen, including a 4:1 power combiner and a traveling wave circuit on sapphire with 100 Ω-mm optimum loads. Using power devices chosen from the matrix being fabricated, a 20 W at X band power combiner circuit will be made initially. The traveling wave amplifier will be simulated, using the properties of power devices from the matrix, and then fabricated after the combiner circuit has been tested. Thermal simulation of the MODFET's on SiC has been done for 10 W/mm heat dissipation, yielding ~10°/W thermal resistance for large pitch distance between gates, and ~ 20°/W thermal resistance for 50 μm pitch.

B. High Power High Efficiency Amplifier Broadband Circuit Design Concepts - Bruce M. Green, Paul J. Tasker

1. Overview

A dedicated high-power amplifier circuit design effort at Cornell began in August 1997 and is growing fast. At present one Ph.D. student and two master's students are working in the amplifier circuits area. A systematic approach is being used to produce a power amplifier design that will meet the ONR requirements (X band, 100 W output power, 60% power added efficiency, linearity, and multi-octave bandwidth). To this end, two short-term (6-12 mos.) and one long term (1+ yrs.) research efforts are underway. The first effort consists of realizing an efficient 6-12 GHz one octave power amplifier using GaN devices. The second effort focuses on high-power characterization of GaN devices to be used in the circuit design. The third, longer term project addresses the use of multi-dimensional traveling wave amplifiers to achieve large bandwidths with high power-added efficiencies. The one-octave amplifier and transistor characterization efforts will give experience in designing power amplifiers at high impedance levels unique to wideband devices. The investigation of traveling wave amplifiers will produce an amplifier topology that will meet the ONR requirements.

2. One Octave Amplifier Design

As a first step in realizing a power amplifier using GaN devices, a hybrid, single octave, ≤ 20 W power amplifier as shown in Figures 1 and 2 is currently under development. Termination of the second harmonic must be used to achieve efficiencies significantly greater than 50%. To date, wideband push-pull operation of the transistors at X band has not been achieved due to the lack of an efficient balun that operates over more than one octave. For this reason, bandwidth of this initial amplifier will be limited to a single octave. Efficient combining of power produced by the gain cells will be obtained using a 4:1 Wilkinson power combiner as shown in the figure.

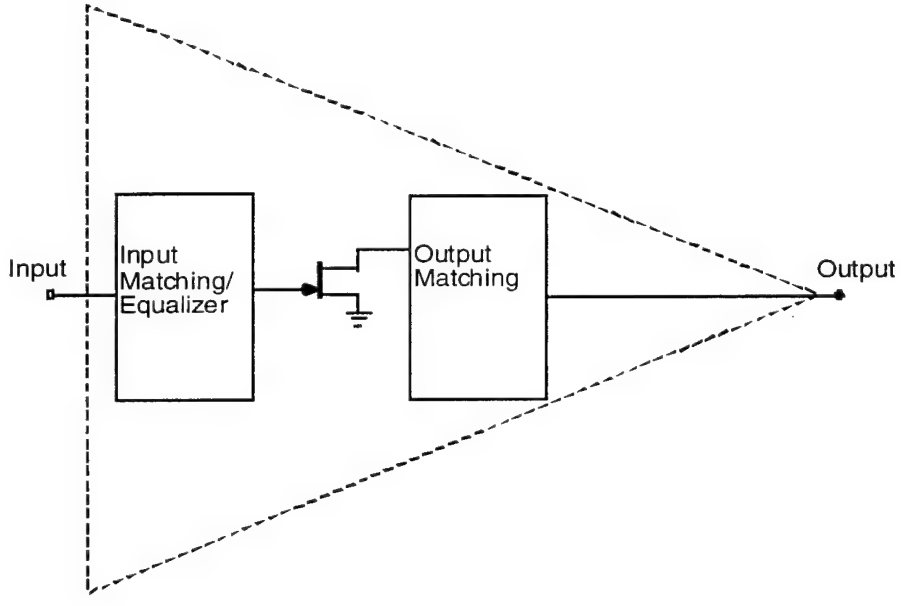

Figure 1. Amplifier gain cell.

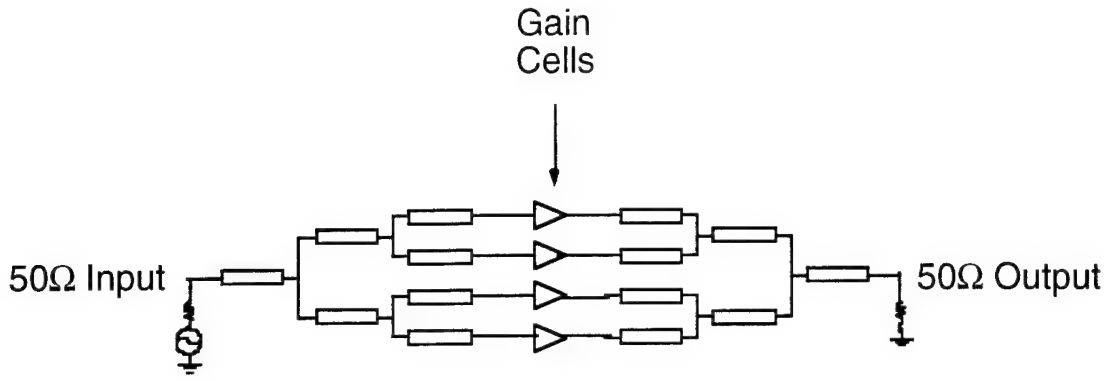

Figure 2. Amplifier topology shown using Wilkinson power dividers/combiners.

Devices The high breakdown voltage of the GaN material affords the design of MODFETS with output impedances in the neighborhood of 50 Ω. In addition, growth of the devices on SiC substrates will allow high power dissipation by the devices. It is expected that 25 W/mm will be achievable with optimized AlGaN/GaN MODFETs on SiC substrates. These MODFETs will have optimum load resistances of 100 Ω-mm.

The first MODFETs used in the amplifier design will be grown on already available sapphire substrates at lower power levels (≤ 5 W/mm) with the same optimum load resistance of 100 Ωmm. The transistor used in the amplifier will be selected by optimizing the number of fingers and gate lengths such that the ≤ 5 W/mm goal is reached. Table 1 shows a matrix of impedance values for different gate finger widths and numbers of fingers. The transistor used in the amplifier design will be chosen from this matrix when it is fabricated and characterized.

	75 μm	100 μm	125 μm	150 μm	200 μm
16 fingers	83.5 Ω	62.5 Ω	50 Ω	42 Ω	31 Ω
12 fingers	111 Ω	83 Ω	67 Ω	56 Ω	42 Ω
8 fingers	167 Ω	125 Ω	100 Ω	83.5 Ω	62.5 Ω
4 fingers	333 Ω	250 Ω	200 Ω	167 Ω	125 Ω
2 fingers	666 Ω	500 Ω	400 Ω	333 Ω	250 Ω

Table 1. Matrix of devices with varying number of fingers and gate width and optimum load resistance for amplifier design based on an normalized optimum load resistance of 100 Ω-mm.

Matching Networks Assuming ideal operation of the devices, a limiting factor in the efficiency of the amplifier is the degree to which the transistor output may be matched to the combining network. Because of the low sheet charge densities used to realize high breakdown voltages in the GaN devices, the f_t of the devices will begin to taper at the high end of the 6-12 GHz range. To compensate for this, the input matching network will have a frequency response that tapers at the

lower end of the 6-12 GHz band thus giving the overall amplifier a flat frequency response. Transmission lines will provide the reactances needed to realize the matching networks over a broad band and at high power.

Substrates In order to effectively dissipate heat from the hybrid circuit components, aluminum nitride (AlN) has been chosen as a substrate material due to its relatively good thermal heat conductivity (1.70 W/cm°K). Plated gold will provide the high conductivity needed for efficient passive components.

3. Power Device Characterization

In order to merge future GaN devices into amplifier designs, large signal characterization of the devices will be needed. This characterization will be performed both at Cardiff University, Wales and at Cornell. Cornell will be expanding its high-power measurement capabilities this year with the acquisition of two electro-mechanical tuners. These will be used in conjunction with the two microwave transition analyzers (MTA's) to provide time domain characterization of the devices.

4. Multi-Dimensional Traveling Wave Amplifier

The use of traveling wave amplifiers (TWA's) to achieve wideband frequency responses is undisputed. However, the dissipation of a backward wave in a dummy load of a traditional TWA severely limits its efficiency. The use of two dimensional traveling wave amplifiers with non-uniform drain line impedances [1,2] are currently being investigated. In the coming year, amplifier topologies using these innovations will be simulated using GaN device properties.

5. Summary

Power amplifier design at Cornell is in its initial phases. In this report, an initial GaN 20 W, 6-12 GHz amplifier was described. Characterization of GaN power devices was described in conjunction with this amplifier. A longer term project involving the realization of 2-D TWA's was also discussed. The actual design and realization of these concepts will take place during the 1997-98 year of the MURI program.

6. References

[1] Houng, S.G., "2-D Distributed Amp Ups Power, Not Load," Microwaves & RF, pp. 139-140.

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C. Thermal simulation of GaN MODFET structures on SiC substrates - Nils Weimann

Because of the high power densities of the GaN devices, thermal aspects have to be included in the device design. For a single device with a microwave output power of 15 W/mm, operated with an efficiency of 60%, the dissipated heat for a 1 mm periphery device amounts to 10 W/mm. SiC and GaN being wide-bandgap semiconductors, devices made of these materials can be operated safely at temperatures of 200°C. The distance between two source fingers (pitch) needs to be small for minimized phase delays, and this is traded off with device heating.

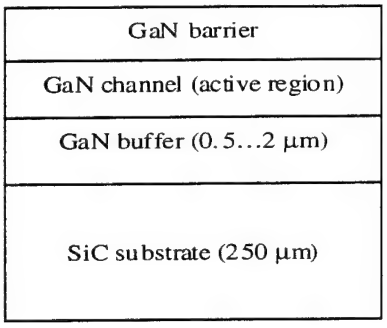

Figure 1: MODFET epi structure

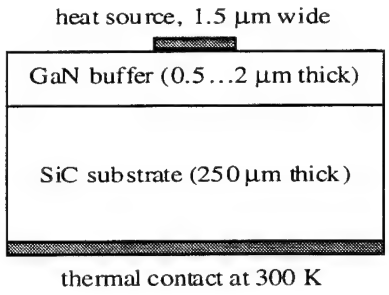

Figure 2: simulated geometry

The surface temperature is simulated for MODFET structures, consisting of a SiC substrate (250 μm thick) and a GaN/AlGaN layer system on top of it (see Figure 1). The thickness of the GaN/AlGaN layer system is determined by the GaN buffer thickness, the AlGaN/GaN layer system is approximated by a single GaN layer. The heat source between source and drain is approximated by a 1.5 μm wide boundary segment on top of the GaN buffer with a constant heat flux, totaling to 10 W/mm (see Figure 2).

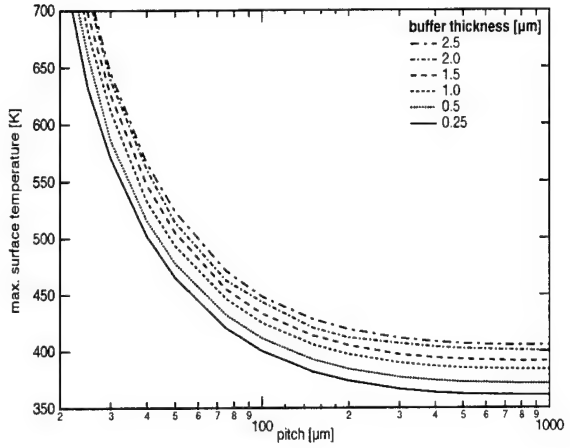

Figure 3: maximum surface temperature

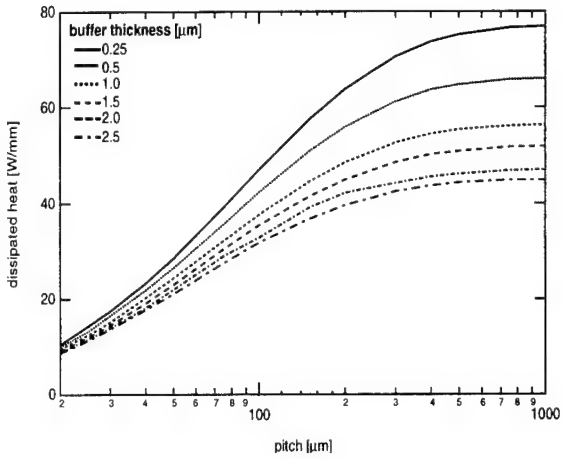

Figure 4: maximum dissipated heat

The thermal conductivities [1] of SiC (5 W/cmK at 300 K) and GaN (1.3 W/cmK at 300 K) are assumed to depend inversely on temperature ($\sim 1/T$). The heat flow equation $-\nabla \cdot k\nabla T = 0$ is solved simultaneously in the two regions, while holding the backside of the substrate at 300 K. The numerical solution of the nonlinear partial differential equation is computed using the PDE toolbox for MATLAB. The maximum surface temperature under the gate vs. pitch for different buffer thickness is shown in Figure 3, and the maximum dissipated heat for a maximum surface temperature is shown in Figure 4.

[1] *Landolt-Börnstein numerical data and functional relationships in science and technology*; edited by O. Madelung and W. Martienssen (Springer-Verlag, Berlin, New York, 1996).

IV. Theoretical Studies

A. Summary - L.F. Eastman

GaN HFET materials design has been carried out, using the C-band computer program to yield ~$1x10^{13}/cm^2$ electron sheet density with 30% Al.

This program will be altered to include the strong piezoelectric effects from the strained AlGaN/GaN structure. Theoretical effort on the design of the complete high power HFET, including deep submicron gate effects, is being made and being compared with device measurements. The severe effect of dislocations on electron mobility has been theoretically evaluated and successfully compared with measurements. Finally, Monte Carlo calculations of electron transport, especially in short devices, have been made for GaN, InN, and AlN.

B. Transistor Materials Design - M. Murphy

There are two tools that are used to model and design transistor structures. The first is a program that performs a simple model approximation on various types of AlGaN/GaN structures. This program determines sheet densities and energy levels as a function of both channel width and spacer width. The channel width offering the highest sheet density is then modeled with a more rigorous program called CBAND. This tool solves the fully quantum-mechanical Poisson and Schroedinger equations simultaneously. Figure 1 shows a typical band diagram for a structure consisting of 40%AlN in the AlGaN barrier, with an 80Å spacer and a 30Å quantum well of GaN. The resulting sheet density is 8.5E12 cm^{-2} .

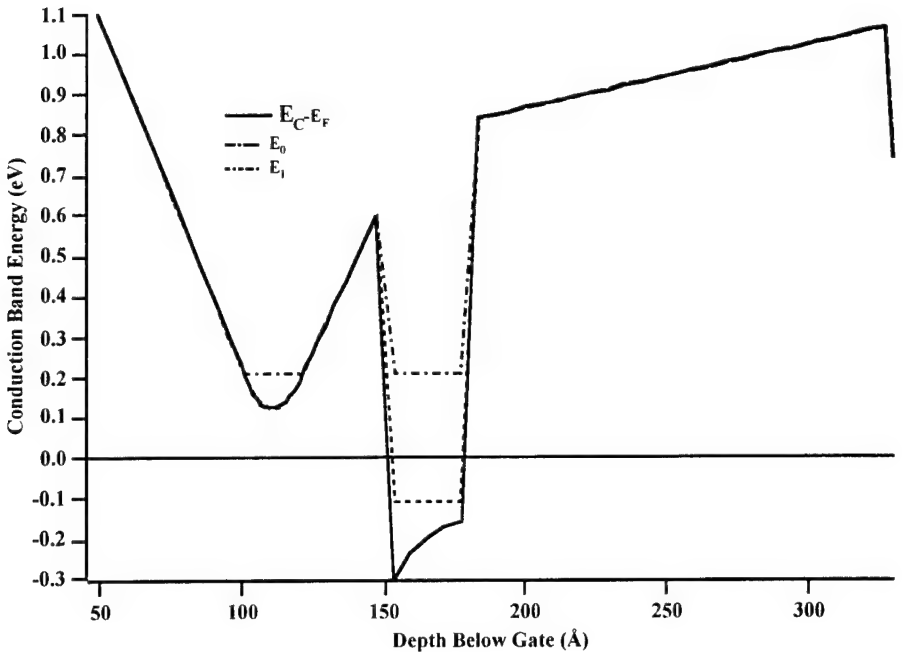

Figure 1. Typical output from CBAND. The structure is $Al_{.4}Ga_{.6}N/GaN/Al_{.4}Ga_{.6}N$. The spacer is 80Å and the channel is 30Å. The resulting sheet density is 8.5E12cm^{-2}.

Several basic transistor layer structures were designed using these techniques. These structures consist of layers containing modest percentages of aluminum nitride, roughly twenty percent. The undoped channel for current flow is created between the AlGaN layer and a layer of GaN. Both of these surrounding layers are moderately to heavily doped with silicon. This design was used for three different transistor growths all with varying silicon doping. All of these layers have been tested for contact and mobility, but none of them were up to specifications. To date these devices have not been further processed.

Several new transistor designs were then modeled. All of the new transistor designs implement double sided doping. This is to ensure that a large (~1E13 cm^{-2}) two-dimensional electron gas (2-DEG) density be present in the channel. This will also offer much better confinement of those carriers in the channel. The final benefit of this scheme is to make sure that all of the carriers are not only quantized but in the lowest energy state, thereby offering the highest kinetic energy possible.

There are three similar designs for this set of trial transistors, none of which contain InN, this is because of the difficulty in deposition. The three transistors are composed of a generous buffer layer (~1-2 microns) of GaN followed by a bottom barrier of AlGaN. This AlGaN layer will be roughly 150 Å thick and contain the lower doped region. Both the doping and AlN content will be varied from transistor to transistor. The doping will be maximized to ensure the largest possible sheet density in the GaN channel while still keeping the conduction band minimum in this region at least .12 eV above the fermi level. This is a very important consideration because we wish to minimize the parasitic carrier transport effects of the barriers.

The next layer is the GaN channel. For this design the optimum channel width is roughly 30 Å. The final region is another 150 Å section of AlGaN, again with varying AlN composition and doping. For both of the doped sections the spacer width has also been varied, from 30 Å to 5 Å.

The reason for the variation in AlN concentration and spacer widths is to determine the effects of ionized impurity scattering on the mobility as well as the difficulties in depositing better barrier materials. There have been many reports that suggest that AlGaN forms micro-cracks if the percentage of AlN is too high. However, the extra AlN will offer better confinement of the 2-DEG. Therefore, if we have to sacrifice the confinement we also have to move the doped region closer to the channel in order to get substantial sheet densities. Therefore the following three designs are proposed.

The first design being 20% AlN in the AlGaN barriers. This means that a maximum sheet density in the channel will be roughly 6.3E12 cm^{-2}. However, to accomplish this and still meet the other requirements of minimizing the parasitic effects of the barriers, we must use a spacer width of 5 Å.

The second design utilizes a barrier with 30% AlN. Because of the much greater confinement (roughly an extra 20%) we hope to achieve a sheet density of 1E13 cm^{-2} while also increasing the spacer width to 10 Å.

The final design will use 40% AlN in the AlGaN barriers. This will boast an increase in confinement nearly 60% more than the first design. This should yield a sheet density of ~1E13 cm^{-2} and allow a spacer width of 30 Å.

By pursuing these designs, we can answer some very important questions about the trade-offs between spacer widths, sheet densities, and mobilities, as well as determine some of the deposition difficulties in achieving high confinement barriers.

After these designs were made, there was much enthusiasm about the possibility of the piezoelectric effect and the proposed ability that no other doping was necessary in these devices. The piezoelectric effect should increase the 2-DEG concentration by a maximum of 5E13 cm^{-2} for AlN on GaN. This value should scale linearly with AlN percentages (courtesy Prof. Asbeck). Our modeling software has been modified to take into account this effect, and further designs will not only include the effect but also help to further prove its existence.

Some designs were made taking into account the piezoelectric effect only. These designs specified that nearly 30% AlN is needed in the barrier to achieve a sheet density of ~1E13 cm^{-2}. So far, we have not yet been able to achieve this increase in carriers due to the piezoelectric effect in our material.

C. Design, Characterization, And Simulation Of High-Voltage, High-Power AlGaN/GaN HFET's - M. S. Shur

This work was performed in collaboration with researchers at APA Optics, Cornell University, the University of Illinois at Urbana-Champaign, and the University of Virginia.

We have reported on the DC and microwave performance of 0.25 micron gate Doped Channel $Al_{0.14}Ga_{0.86}N$/GaN HFETs. We have found a cutoff frequency of 37.5 GHz and a maximum frequency of oscillation of 80.4 GHz. Calculations of the Fermi level position, and a comparison with the expected conduction band discontinuity, confirmed that the channel in these transistors was doped. The DC and microwave characteristics of these devices do not change much with temperature, at least up to 200 °C and 90 °C, respectively [1].

In order to obtain a higher breakdown electric field, we have developed AlGaN-GaN DC-HFETs with offset gates [2]. The breakdown voltage in these devices exhibited a strong dependence on the gate-to-drain separation, and the maximum transconductance increased almost linearly with the

source-to-drain distance. A breakdown field of 1.3 MV/cm was obtained. The offset design also resulted in a reduced gate leakage current.

We have also found a high turn-on voltage (approximately 2.5 V) of the gate-source leakage current in AlGaN/GaN High Electron Mobility Transistors (HEMTs). A larger conduction band discontinuity and a higher electron effective mass (compared to AlGaAs/GaAs HEMTs) lead to a lower gate current and a higher turn-on voltage. The piezoeffect and the doping result in the electron sheet concentration were found to yield 2DEG of the order of 10^{13} cm^{-2} [3]. Calculated results of the band structure as effected by the piezoeffect are shown in figure 1.

In addition, we have reported on new AlGaN-GaN HFETs on SiC substrates. The devices exhibited a current of up to 0.95 A/mm with a stable performance up to 250 °C with the current saturation up to 300 °C. The maximum power dissipation at room temperature was found to be 6 x 10^5 W/cm^2 [4].

We have reviewed recent progress on GaN-based devices for electronic applications in our invited talk to be presented at the European Device Research Conference [5].

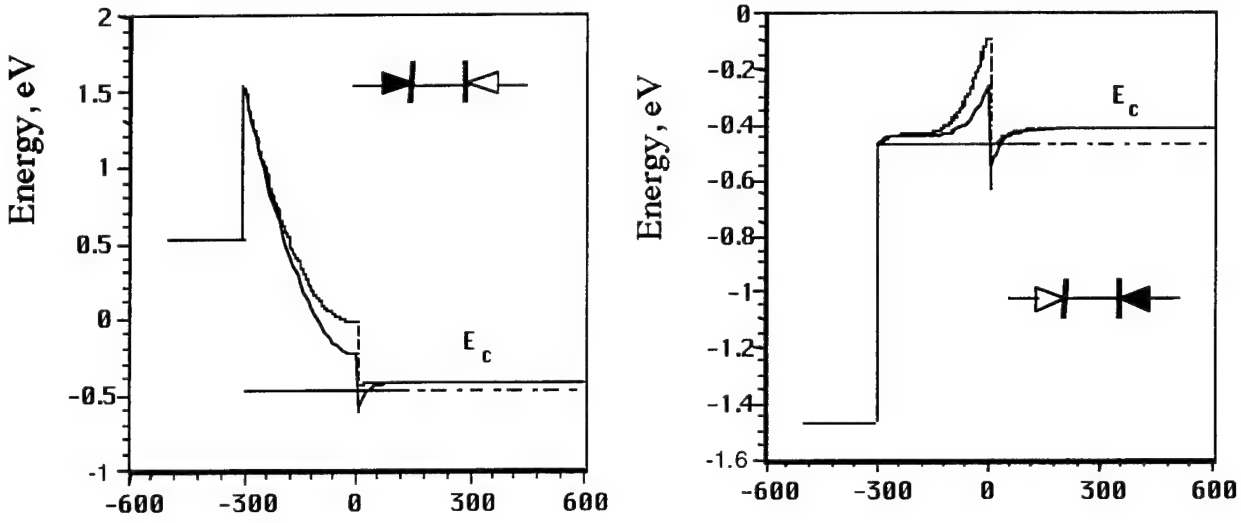

Fig. 1. Calculated band diagrams of the $Al_{0.2}Ga_{0.8}N$/GaN HEMTs accounting for the piezoeffect (solid lines) and neglecting the piezoeffect (dotted lines) at gate voltages -1V (a) and +1V (b). Donor concentration in $Al_{0.2}Ga_{0.8}N$ is 10^{18} cm^{-3}. Also shown is the two-diode equivalent circuit. The equivalent circuit diode controlling the gate current is shown in black [4].

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D. Modeling of Deep Submicron GaN/AlGaN HFETs at Microwave Frequencies for Design of High Power Amplifiers - B. Iniguez and J. Deng

The design of high power microwave GaN/AlGaN HFET amplifiers requires accurate and reliable mixed mode models that should describe both dc and ac characteristics over a large range of applied biases and device currents. The development of such a model presents a challenge [1].

We first addressed this challenge for conventional AlGaAs/GaAs HFETs. Recently, we have been able to demonstrate such a model for the first time.

Under the auspices of this MURI program, we developed such a model for 0.25-micron GaN/AlGaN HFETs that have been described in our papers [1, 2].

We simulated the microwave performance of this transistor and compared it with our experimental data (up to 1.7 W/mm) and started our analysis of the design trade-offs [2]. This included the analysis of the gate length and parasitic series resistance effects on the microwave performance.

[1] T. Ytterdal, Tor A. Fjeldly, Michael S. Shur, S. Baier, R. Lucero, "Complementary Heterostructure Field Effect Transistor Models for Mixed Mode Applications," ISDRS-97, submitted.

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E. Transverse Mobility In GaN - Nils Weimann

Monte Carlo simulations[1] of velocity-field-curves for wurtzite GaN show a low-field mobility of up to 2000 cm^2/Vs. At the start of this program, the measured Hall mobilities for GaN grown by MOCVD or MBE ranged between 100 and 400 cm^2/Vs. To date, the best electron mobility in MODFET structures peaks at 1200 cm^2/Vs, still significantly reduced compared to the theoretical data.

According to our model, this discrepancy can be explained with electron scattering at charged dislocation lines. The threading dislocation density in epitaxial GaN ranges from $10^7 \ldots 10^{11}$ cm^{-2}, depending on growth technique and buffer recipe[2]. In TEM cross sectional micrographs, the threading character of the dislocations in hexagonal GaN can be seen. The dislocation density can be measured by counting the lines in TEM pictures, or by measuring the Full Width at Half Maximum (FWHM) of asymmetric X-ray reflections, e.g. of reflections at the [102] planes, while the edge dislocation density has no broadening effect on the commonly measured [002] reflection-FWHM[3].

While the distorted crystal structure around the threading dislocation lines already leads to electron scattering, it cannot account for the large reduction of the electron mobility. This can be explained by Coulomb scattering at charged dislocation lines, assuming an acceptor-like deep trap at the "dangling bond" of every atom along the dislocation line.

The yellow emission band in GaN is evidence for the existence of a deep trap. The broad FWHM of about .5 eV can be attributed to closely spaced traps with overlap of wave functions at adjacent trap sites. The acceptor-like character of the deep trap 2.15 eV below the conduction band has been shown by pumped Photoluminescence and Deep Level Transient Spectroscopy experiments[4].

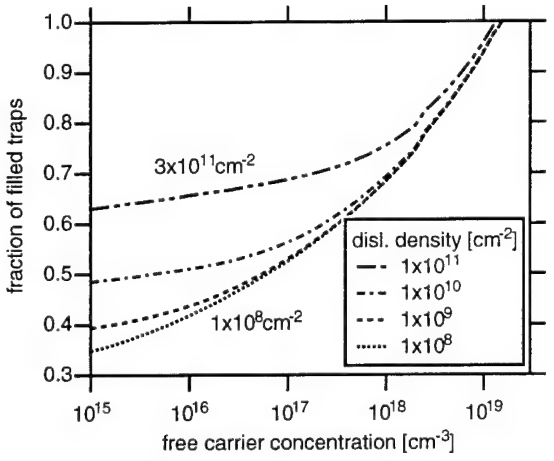

Figure 1: fraction of filled traps vs. free carrier concentration

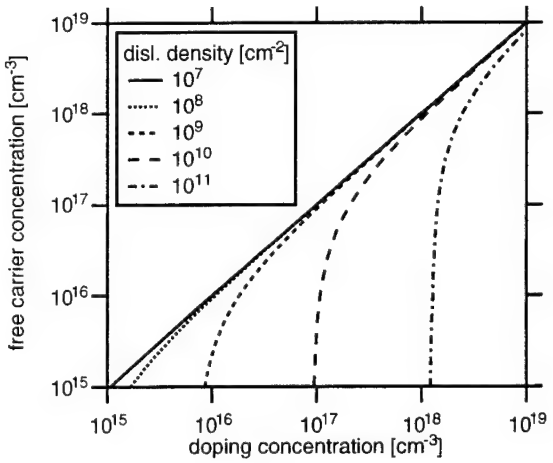

Figure 2: free carrier concentration vs. doping concentration

Using a model developed by Read for the case of germanium[5], and later refined by Schroeter and Labusch[6], the fraction of filled traps can be calculated as a function of doping level. The fraction of filled traps is shown in Figure 1 as a function of free carrier (electron) concentration, and can be converted to the doping concentration necessary for a measured free carrier concentration (Figure 2). The doping range in highly dislocated material is limited by the trapping of free electrons in states at dislocation lines: only the doping range above the steep rise of the curves in Figure 2 is accessible.

Knowing the fraction of filled traps, and thus the charge density on a dislocation line, the transverse mobility component due to scattering at charged dislocations can be computed using an analytical expression developed by Pödör[7]. As shown in Figure 3, the mobility is reduced by scattering at charged dislocation lines for dislocation densities > 10^9 cm^{-2}.

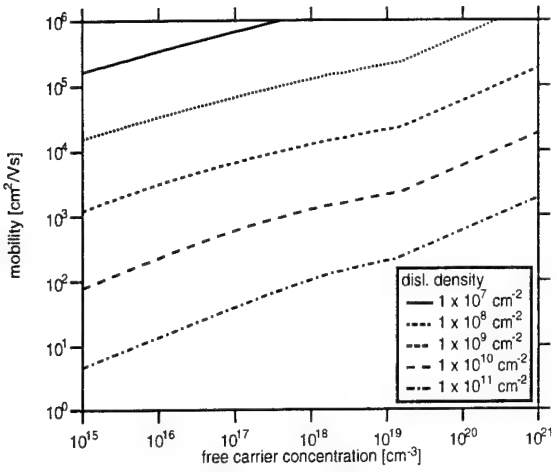

Figure 3: transverse mobility component due to dislocation scattering

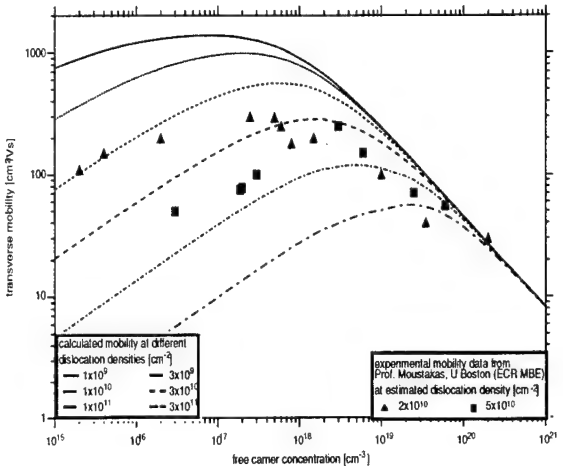

Figure 4: total transverse mobility

The dislocation scattering mobility component can be combined with mobility components from ionized impurity scattering (Conwell-Weisskopf formula[8]) and lattice scattering (constant, 2000 cm^2/Vs). The total transverse mobility shows a maximum at about 10^{18} cm^{-3} electron concentration. Experimental data[9] matches well the predicted mobility (see Figure 4).

Scattering occurs only for electron transport perpendicular to the dislocation lines, vertical current transport is not affected. The band bending around the charged dislocation lines repels electrons from the scattering center, enabling carriers to move unscattered between the depleted regions around dislocation lines. Vertical devices (LED's, lasers, SIT's) can benefit from the superior vertical transport properties in GaN.

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F. Electron Transport in GaN and Related Materials - B.E. Foutz and S.K. O'Leary

The steady-state and transient transport characteristics of a given semiconducting material will ultimately dictate the performance of such a material in a device configuration. In order to establish these transport characteristics, the Monte Carlo simulation approach is often used. We have performed Monte Carlo simulations of electron transport in gallium nitride (GaN), indium nitride (InN), and aluminum nitride (AlN). We report initially on our steady-state results and then on our transient results.

1. Steady-State Electron Transport

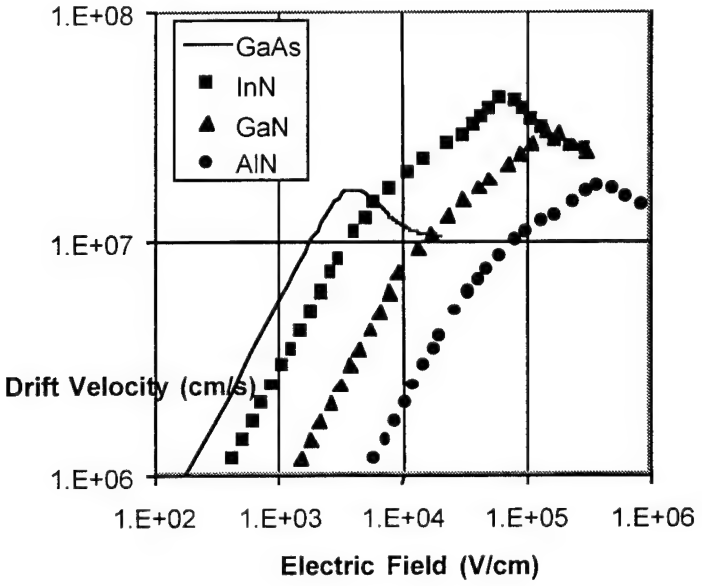


Figure 1: The steady-state velocity-field characteristics associated with GaN, InN, AlN, and GaAs. The GaAs plot is from J. M. Xu, *et. al.*, Appl. Phys. Lett. 49, 342 (1986).

We have determined the velocity-field characteristics of wurtzite GaN, InN, and AlN, using our ensemble Monte Carlo approach. In Figure 1, we contrast the characteristics associated with these materials with that associated with GaAs. For all cases, we set the temperature to 300 K and the doping concentration to 1 x 10^{17} cm^{-3}. We note that InN exhibits an extraordinarily high peak drift velocity, around 4.3 x 10^7 cm/s, at an electric field of around 67 kV/cm. This represents one of the highest peak drift velocities ever reported for a III-V semiconductor. The sharp peak exhibited in the InN velocity-field characteristic contrasts dramatically with the broad peaks predicted for the GaN and AlN cases; in GaN, a peak drift velocity of 3.1 x 10^7 cm/s occurs at an electric field of around 150 kV/cm, while for AlN, a peak drift velocity of 1.8 x 10^7 cm/s occurs at an electric field of 400 kV/cm. It is noted that the drift velocity of InN exceeds that of GaN, or at the very least is close to that of GaN, for the entire range of electric fields considered, the saturation drift velocities of InN and GaN being comparable. While GaAs exhibits a much higher low-field mobility, for comparable selections of temperature and doping, its peak drift velocity is only 1.7 x 10^7 cm/s, this peak occurring at a much lower electric field, 3.5 kV/cm. Given that the saturation drift velocity of

GaAs is of the order $1.0 \cdot 10^7$ cm/s, it is clear that both InN and GaN are more suitable for high speed device applications. AlN itself may find its own specialty application in high power devices, considering that its peak drift velocity, as well as its saturation drift velocity, exceed those exhibited in GaAs.

It is well known that temperature plays a decisive role in influencing the velocity-field characteristics of semiconductors. The dependence of the velocity-field characteristic of GaAs on temperature is well known. The peak drift velocity and the saturation drift velocity are found to decrease substantially with increased temperatures. Quantitatively, for a doping concentration equal to $1 \cdot 10^{17}$Êcm^{-3}, it is seen that the peak drift velocity at a temperature equal to 150 K is $2.2 \cdot 10^7$ cm/s, while that which occurs at 500 K is only $1.0 \cdot 10^7$ cm/s at 500 K; see Figure 2. The corresponding saturation drift velocity changes from $1.4 \cdot 10^7$ cm/s at 150ÊK to $0.7 \cdot 10^7$ cm/s at 500 K. By way of contrast, the peak drift velocity associated with GaN only changes from $3.2 \cdot 10^7$ cm/s at 150 K to $2.7 \cdot 10^7$ cm/s at 500 K, the corresponding drift velocity only changing from $2.6 \cdot 10^7$ cm/s at 150 K to $2.2 \cdot 10^7$ cm/s at 500 K; see Figure 3. It is also seen that while the velocity-field characteristic associated with GaAs exhibits a dramatic change in form with variations in temperature, this is not observed for the GaN case. Similar results are found for InN and AlN.

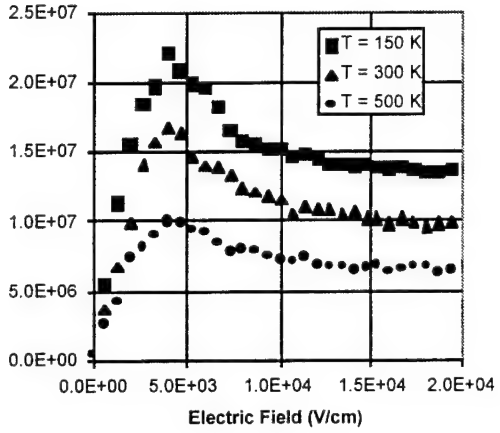


Figure 2: The steady-state velocity-field characteristic associated with GaAs at various temperatures.

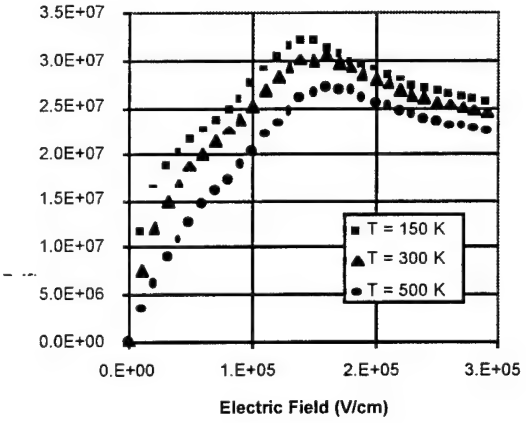


Figure 3: The steady-state velocity-field characteristic associated with GaN at various temperatures.

As with temperature, doping does not play as large a role in influencing the velocity-field characteristic of GaN as it does in GaAs. In particular, while the velocity-field characteristic associated with GaAs changes dramatically with dopant concentrations greater than 1×10^{16} cm^{-3}, for the case of GaN the dopant concentration must be in excess of 1×10^{18} cm^{-3} before substantial modifications in the velocity-field characteristic occur; see Figure 4. Similar results are found for InN and AlN.

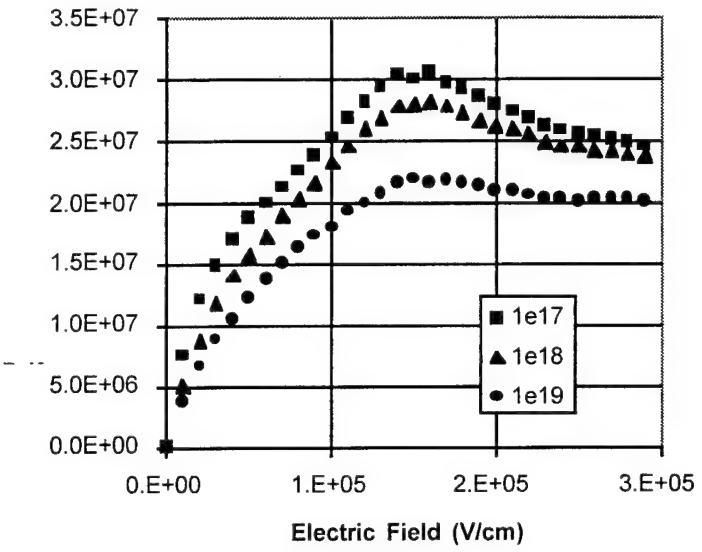


Figure 4: The velocity-field characteristic associated with GaN at various doping concentrations.

Compensation substantially modifies the velocity-field characteristics of a semiconductor. We are currently investigating how compensation modifies the velocity-field characteristics of GaN, InN, and AlN. In Figure 5, we plot the velocity-field characteristic associated with GaN for variation compensation ratios, where the electron concentration is set to 1 x 10^{17} cm^{-3} in all cases; the compensation ratio $\gamma = N_a/N_d$ where N_a and N_d denote the concentration of acceptors and donors, respectively. We see that the peak drift velocity decreases from 3.0 x 10^7 cm/s to 2.6 x 10^7 cm/s as γ ranges from 0.0 to 0.9. The effect is even more pronounced when the electron concentration is set higher.

2. Transient Electron Transport and Overshoot Effects

As device dimensions shrink, short channel effects, such as electron velocity overshoot, become more important. Velocity overshoot occurs when the electric field changes faster than the relaxation time of the electron distribution. During the time it takes for the electron distribution to return to steady-state, the transient drift velocity can exceed, by a factor of three or more, the steady-state drift velocity. These transient effects typically last for several picoseconds, which translates into several tenths of a micron when the velocity verses time curve is integrated. Our approach is to study and characterize these effects though a Monte Carlo electron transport simulator. During this first year of work, it has been shown that the nitride materials potentially demonstrate velocity overshoot and transient effects even more pronounced than those that occur in GaAs. In the nitrides, however, these effects occur at much higher applied biases than in GaAs. Therefore, we expect these effects to be important in high power, high frequency devices, such as those needed for this project.

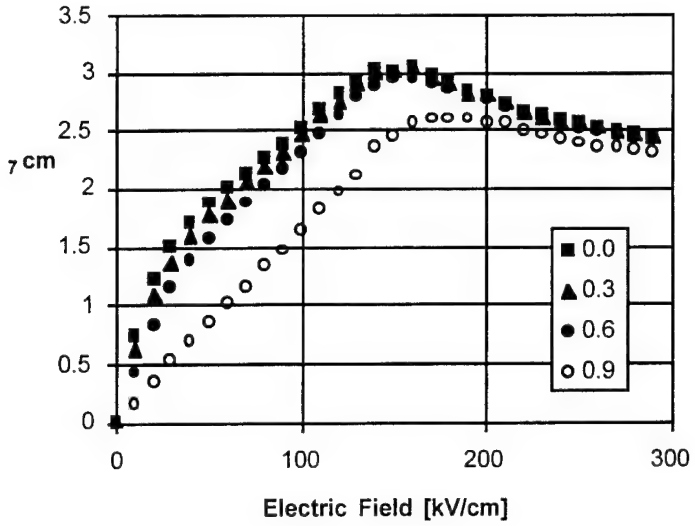


Figure 5: The velocity-field characteristic associated with GaN at various compensation ratios.

In Figure 6, we examine velocity overshoot in InN, GaN, AlN, as well as GaAs. In all cases we set the temperature to 300 K and the electron doping concentration to 1 x 10^{17} cm^{-3}. To provide a reasonable means of comparing transient effects among the materials, the electric field is increased from 0 kV/cm to twice the peak field for that particular material. Note that the overshoot effects in InN have a higher velocity and extend over greater distances than all the other materials. When the field is increased to 600 kV/cm in InN the peak velocity increases to 1.2 x 10^{8} cm/s while the overshoot effects shorten to a distance of 0.1 micron. These results suggest that using InN or GaN channels in field effects transistors should enhance performance in GaAs based counterparts. These results are presently being prepared for publication [4].

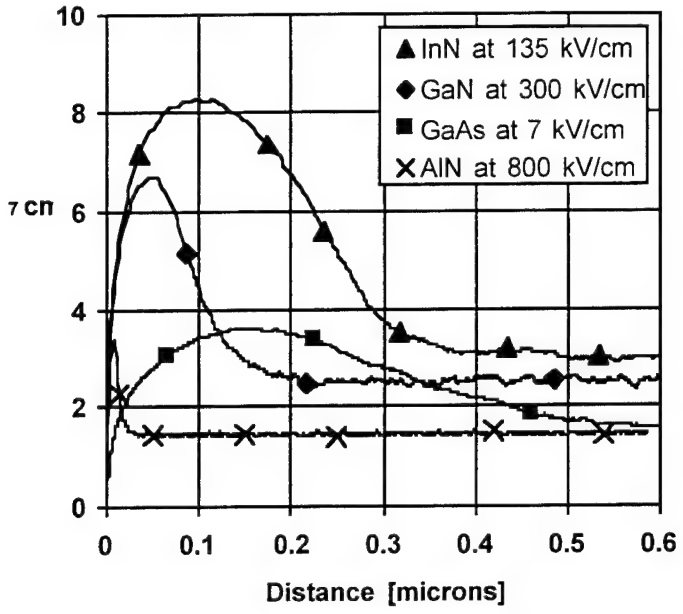


Figure 6: Comparison of transient effects in the materials under study.

In Figure 7, we examine the effect of increasing the applied field from zero to a variety of final field strengths. In this case, the material under study is GaN which demonstrates a peak field value of 150 kV/cm. When the applied field is increased from zero to a value below the peak field, very little or no overshoot occurs. As the final field strength is increased to a value above the peak field, overshoot begins to occur. Just above the peak field, we find that the peak overshoot velocity is not very high. For example, at 200 kV/cm, the maximum overshoot velocity is less than 5×10^7 cm/s. However, the distance over which the overshoot extends is quite large, approximately 0.35 microns in this case. As the field strength is increased further, both the peak overshoot velocity increases and the time for overshoot relaxation decreases. A theoretical understanding of this effect is currently being investigated. These results were presented in a publication [1].

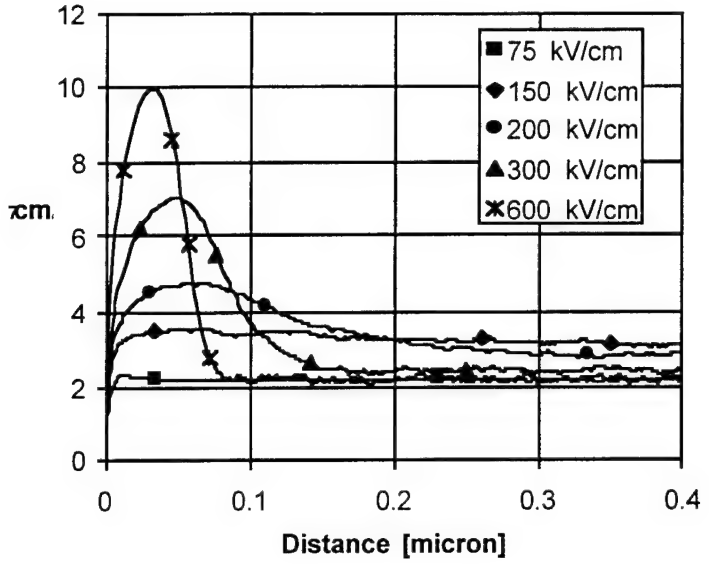


Figure 7: Velocity overshoot in GaN as the electric field is increased from 0 kV/cm to a final field strength.

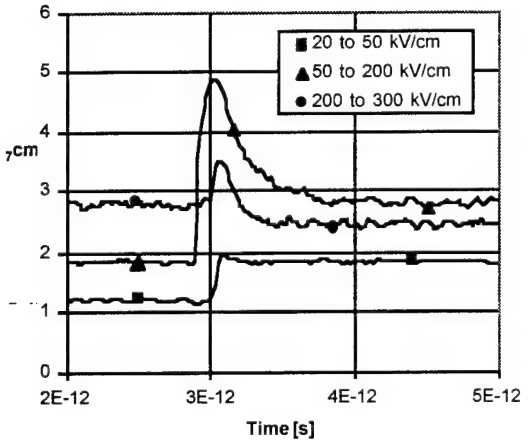


Figure 8a: Overshoot as a function of increasing applied field.

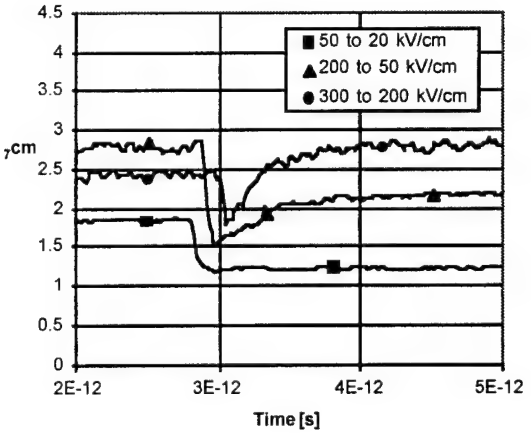


Figure 8b: undershoot as a function of decreasing applied field

We have also studied overshoot effects when the initial electric field is different than zero. This is important, for example, in FET design, since electrons may be entering the channel with a non-equilibrium energy distribution. We find that overshoot effects can be categorized into three cases. First, we find little or no overshoot effects when abrupt changes in the field occur below the critical field (the field at which the peak drift velocity occurs, 150 kV/cm in GaN for example). This can be explicitly seen in Figure 8a with the curve that is labeled "20 to 50 kV/cm". Second, when the

field is below the critical field, and is abruptly increased to a field above the critical field, the most pronounced overshoot effects occur. This can be seen for example in the case when the field electric field is increased from 50 kV/cm to 200 kV/cm. Finally, changes in the field above the critical field lead to only small overshoot effects, as can be seen when the field is increased from 200 kV/cm to 300 kV/cm.

When the field is abruptly lowered velocity undershoot occurs as can be seen in Figure 8b. In these cases however, the magnitude of this undershoot effect is not as great as in the overshoot case. A manuscript of these results is presently being prepared [5]. An understanding of these results will be explored in the next section.

We have found that understanding how the electron distribution function behaves is the key to understanding the transient transport properties of compound semiconductors. Specifically, in Figure 9 we show the electron distribution function of GaN. We find that at low fields the distribution remains narrowly peaked and has a low mean energy. However, as the applied field is increased past the peak field (150 kV/cm in GaN), the electron distribution spreads dramatically in the gamma valley. Now we can use this understanding to explain the dependence of overshoot on changes in the applied field described in the previous section. Large overshoot effects are only observed if the initial electron distribution is narrow and the final distribution is broad. It takes some time for the electron distribution to broaden. It is during this time that the large velocity overshoot is seen. The only curve in Figure 8 that this applies to is when the field is increased from 50 to 200 kV/cm. In all the other curves the initial distribution is broad or both the initial and final distributions are narrow.

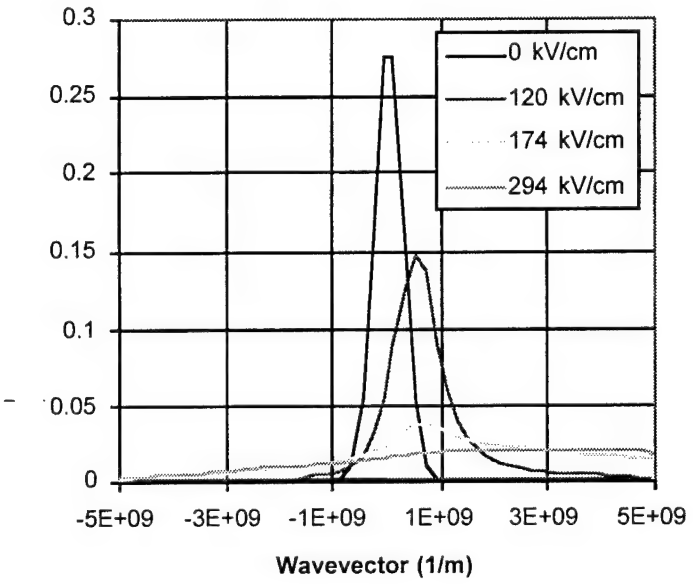


Figure 9: Electron distribution at different field strengths i GaN. As the applied field is increased higher than the pea field (150 kV/cm), the electron distribution broadens considerably.

3. Future Work

1. To determine the effect of some of the lesser-known parameters on the velocity-field characteristics of GaN, InN, and AlN, we have started to examine the sensitivity of our results to variations in these parameters. Preliminary results show that it is only the saturation drift velocity that is affected by these variations in parameters. These results will be featured in a publication that is presently being prepared [6].

2. There is currently no good analytical theory that describes the transient effects demonstrated by our Monte Carlo simulator. We are currently working on an analytical model to describe this behavior.

3. We have also begun to examine the role that the piezoelectric effect has on device design. The piezoelectric effect can enhance electron concentrations at heterostructure boundaries and shift conduction and valence band shapes. We believe an understanding of the stresses and strains at the heterostructure boundary will allow us to modify our current device models to include the piezoelectric effect.

4. In MODFETs and quantum well transistors, where 2-D transport is important, mobility values as high as 10,000 $cm^2/V\text{-}s$ at 77 K have been measured (R. Gaska, J. W. Yang, A. Osinsky, Q. Chen and M. Asif Khan, A. O. Orlov, G. L. Snider, and M. S. Shur, "Electron Transport in AlGaN-GaN Heterostructures Grown on 6H-SiC Substrates," submitted for publication). This is much higher than predicted for bulk GaN (about 3,000 $cm^2/V\text{-}s$ at 77 K). It is currently uncertain why mobility values in the 2-D gas are so much higher than those predicted for bulk material. It is hoped that simulations of the 2-D gas will allow us to predict the behavior of the AlGaN/GaN system. The knowledge gained will be used in device design.

4. Publications

[1] B. E. Foutz, L. F. Eastman, U. V. Bhapkar, and M. S. Shur, "Comparison of High Electron Transport in GaN and GaAs," Applied Physics Letters, Volume 20, pp. 2849, 1997.

[2] U. V. Bhapkar and M. S. Shur, "Monte Carlo calculation of velocity-field characteristics of wurtzite GaN," Journal of Applied Physics, in press, 1997.

[3] S. K. O'Leary, B. E. Foutz, M. S. Shur, L. F. Eastman, and U. V. Bhapkar, "Electron Transport in Wurtzite Indium Nitride," submitted for publication.

[4] S. K. O'Leary, B. E. Foutz, M. S. Shur, L. F. Eastman, and U. V. Bhapkar, "Electron transport in indium nitride and gallium nitride," IBM Poster Day at Rennselaer Polytechnic Institute, June 18, 1997.

[5] B. E. Foutz, S. K. O'Leary, M. S. Shur, L. F. Eastman, and U. V. Bhapkar, "Velocity Overshoot and Ballistic Electron Transport in the Nitrides," in preparation.

[6] S. K. O'Leary, B. E. Foutz, M. S. Shur, L. F. Eastman, and U. V. Bhapkar, "Electron transport in indium nitride and gallium nitride: A Sensitivity Analysis," in preparation.

V. Wide Bandgap Semiconductor Materials Synthesis

A. Summary - L.F. Eastman

SiC bulk crystal wafers have been grown by Northrop Grumman, and supplied to Cornell. These are SiC-4H wafers for the most part, useful for the vertical FET fabrication. A few high resistivity (up to 10,000 Ω-cm) 4H wafers have been supplied, and V-doped 6H semi-insulation wafers will be supplied. Novel means of rapid growth bulk GaN at reduced temperature and pressure have been undertaken, yielding small crystals. Using larger seeds, larger diameter boules will now be grown. FET layers have been grown by MBE on sapphire, yielding mobility values up to ~300 cm^2/V-S during research on different nitrogen sources. OMVPE growth on both sapphire and SiC has been carried out, yielding low net donor densities from C(V)-measurements. Finally, high resolution characterization of epitaxial GaN has been initiated following development of sample preparation.

B. SiC Material Preparation - R. C. Clarke, S. Sriram

This program has been slow in starting due to contractual issues. Northrop Grumman have now completed negotiations and the documents are with Cornell University for signature.

In the abscence of a contract Northrop Grumman has supplied approximately 50cm^2 of 4H-SiC polished wafers consisting of both n+ conducting material and high resistivity undoped wafers.

Northrop Grumman is the leader in the development of high resistivity and semi-insulating SiC substrates for high frequency power device performance and has already produced state-of-the-art quality, 1.5-inch diameter 4H- and 6H-SiC substrates with controlled electronic properties (Figure 1).

Attainment of high resistivity behavior in SiC substrates was first demonstrated by Northrop Grumman and forms the basis of the high frequency performance demonstrated by our devices. Our development of high resistivity SiC derives from the fact that for devices and circuits operating at microwave frequencies, a key requirement is the use of an electrically passive, preferably semi-insulating, substrate which exhibits low dielectric loss and inhibits device parasitics. ***In this regard, Northrop Grumman has achieved several industry "firsts" including demonstrations of semi-insulating 4H -and 6H-SiC crystals and substrates at diameters up to 1.5-inch, exhibiting room temperature resistivity above 10^{15} ohm-cm and $>10^7$ ohm-cm at 250 C, as shown in Figure 2.*** This technology relies on the compensation of shallow electrically active impurities by a deep-level impurity such as VANADIUM or other suitable thermally stable defect center, a technique first employed by Northrop Grumman in the development of high resistivity 6H-SiC, under an Air Force program (Contract No: F3315-92-C-5912) to develop

field effect transistors (MESFETs) operating at frequencies up to X-band. A co-development of this work has been the attainment of high purity 4H-and 6H-SiC crystals with as-grown resistivity > 5000 ohm-cm without intentional deep-level doping. ***These SiC materials advances pioneered by Northrop Grumman have led to SiC MESFETs with as much as four to six times the power density of GaAs at X-band operating frequency.*** The focus of the future effort is to control and reduce defect density of these crystals while improving the uniformity and yield of high resistivity wafers for each boule.

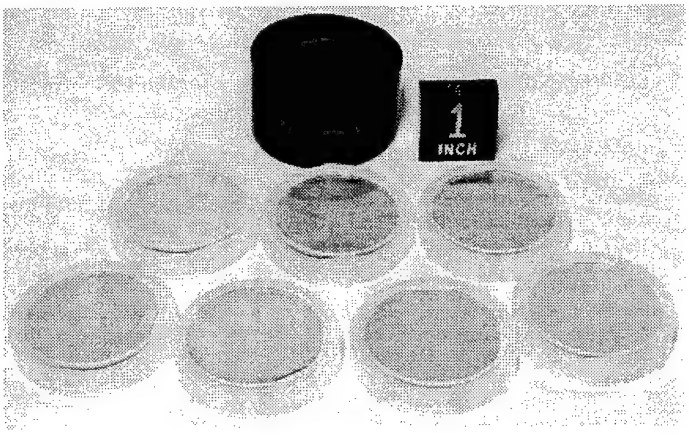


Figure 1 High resistivity SiC substrates

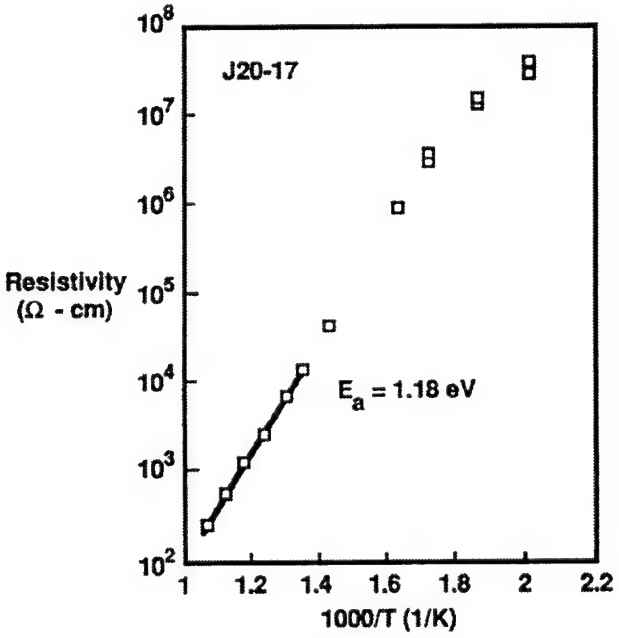


Figure 2 Semi-insulating behavior in 4H-SiC crystals >10^7ohm-cm @ 250C.

C. GaN Bulk Crystal Growth - A. Ruoff

The purpose of this project is to grow large boules of high quality of GaN.

The phase diagram for GaN is shown in Fig. 1.

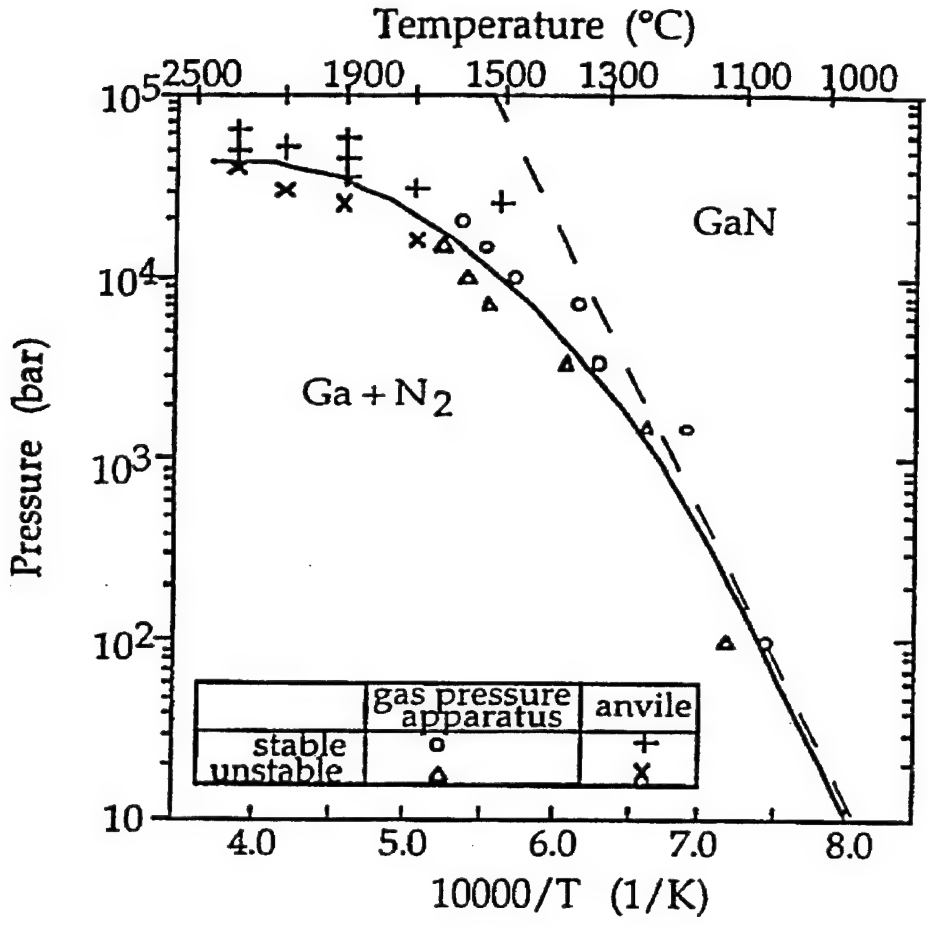


Figure 1 Phase diagram for GaN

According to Porowski, the Gibbs free energy of formation for the reaction is DG_{∞} = -157,700 + 135.65 T. Hence at one atmosphere, DG∞=0 at T=1162.5K, the GaN equilibrium decomposition temperature at one atmosphere. GaN will decompose below 900∞C at one atmosphere and forms Ga and N_2. Below this temperature, GaN is stable with one atmosphere of N_2. However, the kinetics for its formation is very slow. Porowski noted that by increasing the pressure, the decomposition temperature could be raised. His group was able to grow mm size crystals at 1400∞C and 12kbar. But the kinetics was still too slow for practical growth. Higher temperature would mean higher pressure and more expensive apparatus. To circumvent this problem, we began a program using solvents.

Experiments were carried out with two types of solvent (1) liquid Ga-M, where M is a metal and (2) Ionic solvent. We also used nitrogen-containing reactants other than N_2 to avoid the kinetic problem of breaking the triple bond of N_2.

1. Ga-M solvent method

Ga-M alloys dissolve much more N_2 (M=Na, Li and Mg) than Ga itself. We have shown that metal alloys solvents promote crystal growth reactions, such as:

To illustrate how such alloys solutions affect the reaction, we give the phase diagram of Ga-Li, shown in Figure 2.

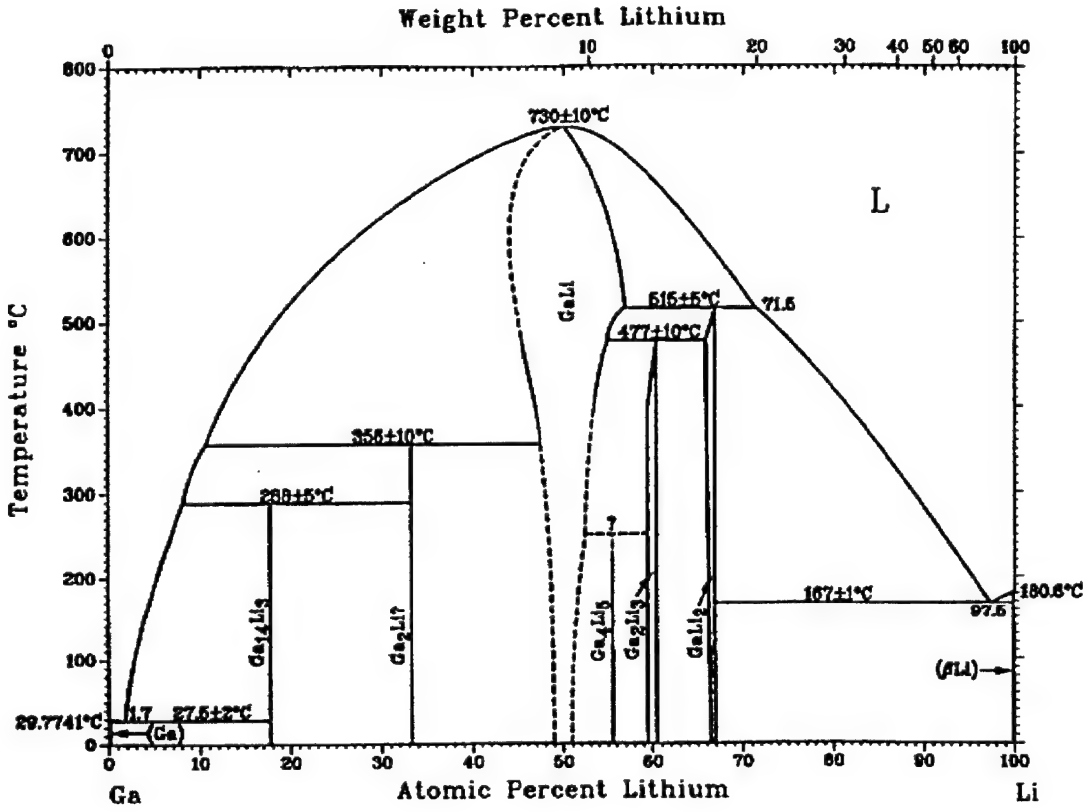


Figure 2. Phase Diagram of Ga-Li

Compound formation below the liquid phase illustrates the attraction of Ga to Li. Figure 3 shows atoms on the surface of GaN.

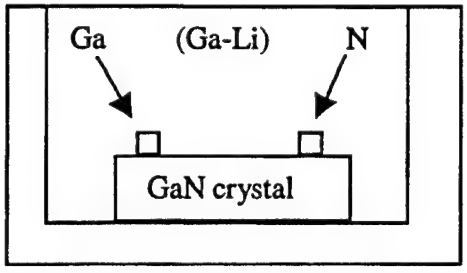


Figure 3. Schematic of atoms on surface of GaN

The environment of the Ga atoms on the interface with the Ga-Li liquid is very much different than on a GaN surface in a vacuum, since the Ga is strongly attracted to Ga-Li solution. Likewise, nitrogen is quite soluble in the Ga-Li solution so it is also strongly attracted to the solution. Thus these atoms have higher mobility and can move more rapidly on the surface at a given temperature than they could in a vacuum. This motion is required so that atoms can align themselves at optimal sites on a surface to produce a good crystal. Without using a seed, transparent GaN crystals of 250mm size were grown. They showed excellent X-ray patterns and a very strong Raman peak. Our next step will be to grow GaN on a seed.

2. Ionic solvent reaction-growth

For ionic solvent reaction-growth, we use the reaction shown below:

Reaction was performed in a LiCl solvent which was heated above its melting temperature. With this procedure, 100mm GaN crystals have been produced at 650∞C and 1 atmospheric pressure.

As before, consider the Ga and N atoms sitting on the surface, the Ga is attracted to Li in the solvent as already shown in Figure 2. The N is clearly attracted to the solution since the stable compound Li_3N exists.

3. Gas Flow Reaction

In experiments carried out to date, rapid growth of GaN crystals (10mm/min) was obtained at pressure near to one atmosphere. We have designed a new flow chamber which is under construction. This will utilize a seed for growing large single crystals. Our initial expectation is 1 cm in diameter within this system. This system should be in operation by the end of October and the design for a larger system is on the drawing board.

4. AlN Single Crystal Growth

As we mentioned before, we are also working on growing AlN single crystal. Since AlN has a much higher decomposition temperature (ª2400∞C), crystals can be grown directly from the gas phase at or near to 1 atmosphere pressure. We began the designing the high temperature furnace in July. The components are now being made and the furnace should be in operation during October. An experiment on growing AlN single crystal is going to start in October.

From the knowledge gained and the developments of the past year, we are confident that we will succeed in growing 1-2cm diameter boules of AlN and GaN. The techniques being work for GaN may be extended (we do not know if it can yet) to AlN which would make the growth temperature much lower and hence the cost lower.

5. Characterization

In another project in our laboratory, techniques have been established for making Raman studies and X-ray rocking curve measurement for these crystals (down to the limit of perfect crystals). Hence rapid method of crystal characterization will be available to us.

D. MBE Growth Of GaN For FET Application - W.J. Schaff, M. Murphy, T. Eustis

Four areas were pursued during this first year.

1. Optimization of GaN growth on sapphire

2. Growths of GaN transistor structures.

3. Initial growths of GaN on 4H SiC

4. Characterization of a new remote RF plasma atomic nitrogen source

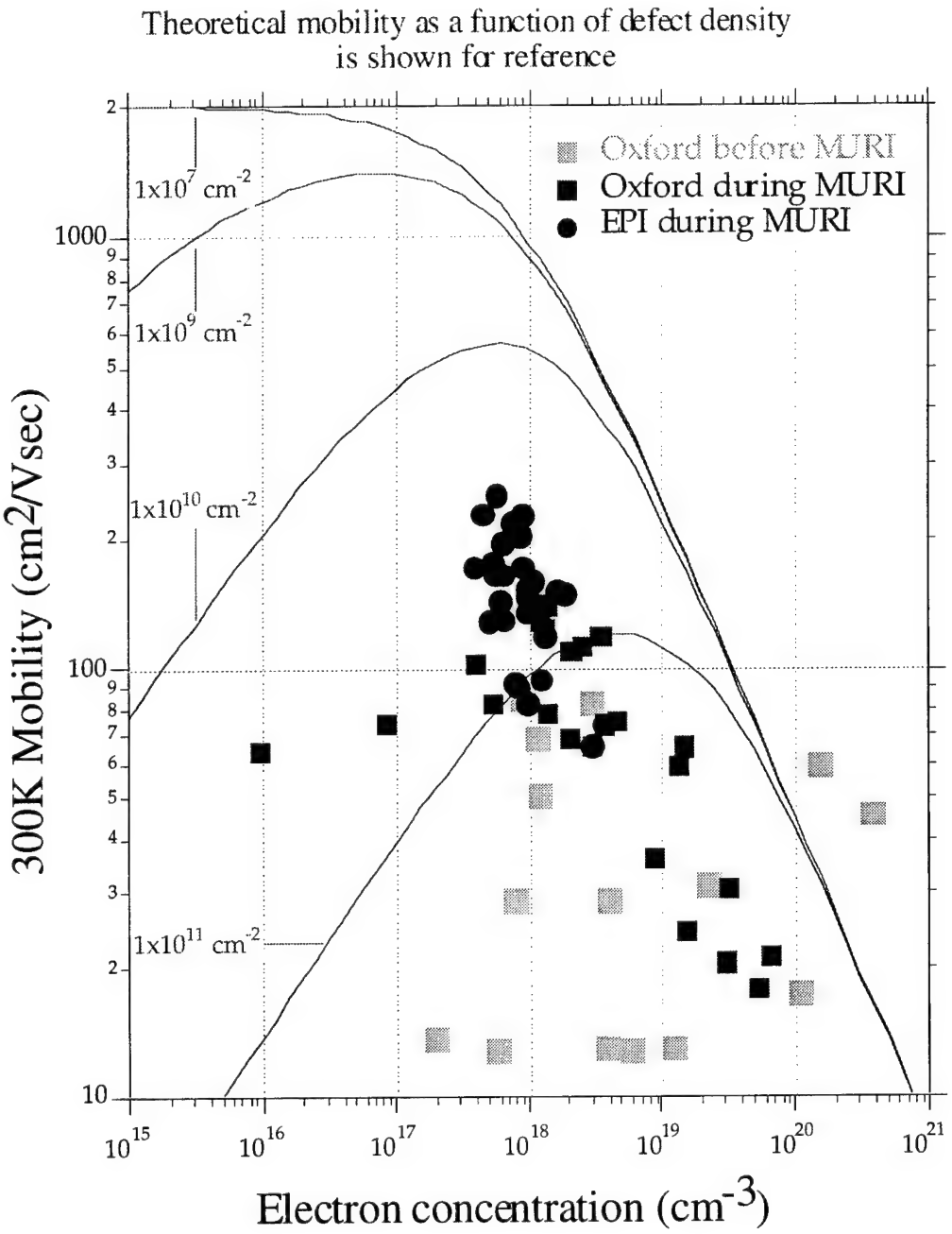


Figure 1 300K mobility of GaN:Si before and during the MURI program using Oxford and EPI RF sources of atomic N. The theoretical mobility is described in Section IV-E.

Efforts to improve MBE growth of GaN have shown significant progress during this first year. The focus of these efforts is optimization of the nucleation layer on sapphire. Evaluation of GaN for transistor applications was primarily through Hall mobility measurements. The best mobilities obtained during this program came from using GaN nucleation layers grown at low substrate temperatures relative to temperatures used for growth of higher quality GaN layers which follow. Significant improvement in growth rates were also obtained by using a more efficient source of atomic nitrogen.

A summary of MBE mobilities for GaN:Si obtained prior to, and during, this program are seen in Figure 1. The early mobilities obtained with the Oxford Applied Research CARS-25 remote RF plasma source of atomic N are among the lowest values due to use of poor nucleation layers. Progress in nucleation layer development took place during this past year as seen in Figure 1. Higher mobilites were obtained as a result of lower defect densities which produced less scattering. The theoretical curves developed during this year are also shown. The effect of defects on mobility are clear. Highest mobilities require lowest defect densities.

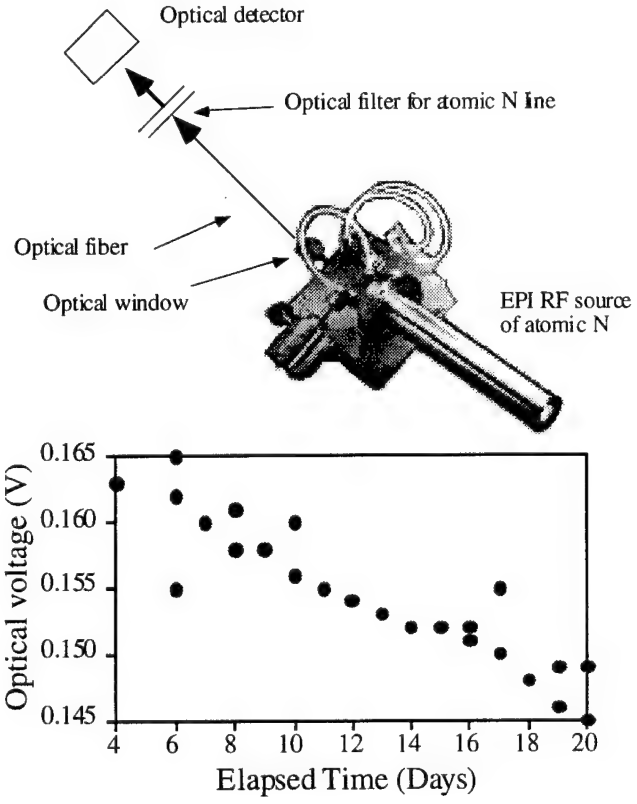


Figure 2 Degradation of optical voltage corresponding to atomic nitrogen

A new form of remote RF plasma source has been installed. A Uni-bulb source from EPI uses one piece construction for improved atomic N generation efficiency. In a few dozen growths, it has been used to reliably grow GaN at rates of 0.6μm/hr compared to a maximum from the previous source of 0.2μm/hr. Mobilities are also higher. For doping of $1x10^{18}$ cm^{-3}, the EPI source produces 300K mobilities between 200 and 300 $cm^2/Vsec$, while the previous source could not grow materials with mobilities beyond 160. Both sources, however, exhibit an undesirable degradation in performance over a time period as short as one month of continuous use. We think we can explain this behavior based on a model of PBN liner erosion.

An optical signal proportional to atomic nitrogen concentration is obtained by viewing the optically transparent PBN liner with an optical fiber connected to a narrow bandpass filter centered at 750nm in front of a detector. This signal has been plotted for the EPI source which was installed in June. It can be seen in Figure 2 that the optical signal intensity falls with time. It is thought that the reason for this fall is due to decreased atomic nitrogen generation efficiency. The reason for the fall in efficiency is because of erosion of the PBN liner which results in dark streaks thought to be boron around the inside perimeter of the PBN liner. A sketch of the liner as seen in the Oxford source is seen in Figure 3.

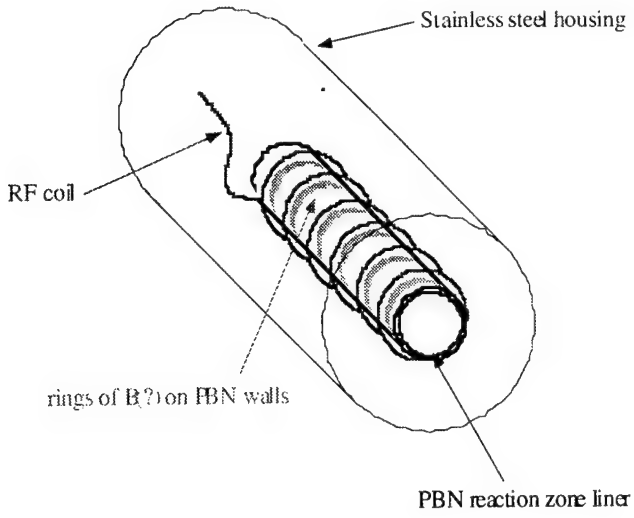


Figure 3 Sketch of PBN liner in Oxford RF source showing dark rings

The best reproducible buffer layer recipe was found to require two ingredients - low growth rate, and high temperature anneal. Nucleation layers are initiated at low growth rates, and growth rate is ramped up to 0.2μm/hr. Anneal at thermocouple temperatures near 1200°C for 15 minutes to 1 hour is then performed prior to lowering the substrate thermocouple temperature to 973°C for epitaxial growth. When these steps are followed, the RHEED image during the growth of the doped layer quickly becomes very streaky, and clear Kikuchi lines are seen. These RHEED patterns are the closest to those of GaAs for GaN growth in this lab. Other growth conditions produce RHEED with different magnitudes of spotty content.

A graphical representation of the growth recipe for GaN on sapphire is shown in Figure 4. It is superimposed on the Ga desorption data taken by a residual gas analyzer located in a furnace port. Approximately 2 hours is dedicated to producing an optimum nucleation layer. The substrate is nitridized for 3 minutes at high temperature, then growth takes place at low temperature while starting at a low growth rate. After a nucleation layer is established, the layer is annealed at high temperature. After anneal, GaN is then grown for device or characterization applications.

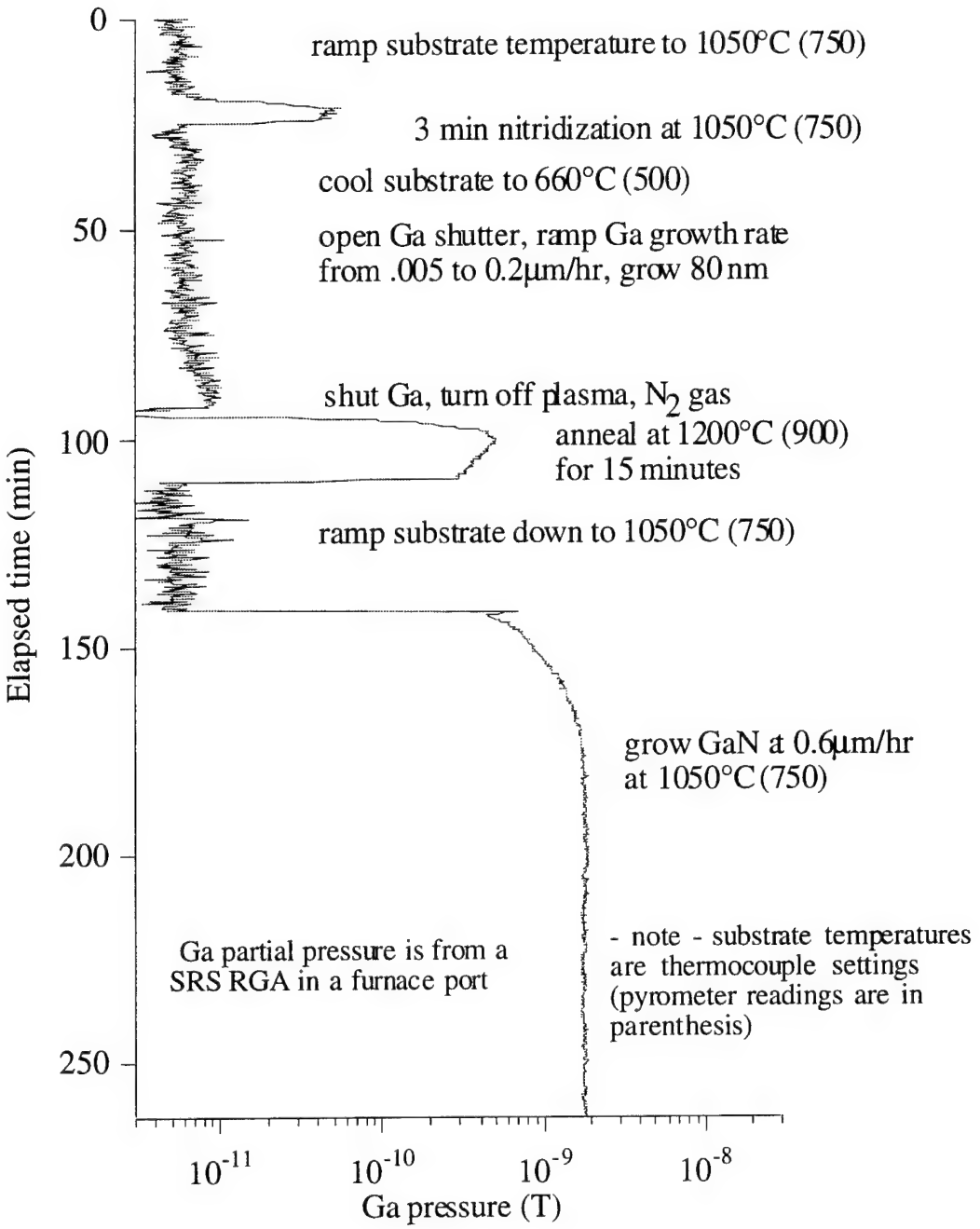


Figure 4 Growth recipe superimposed on Ga desorption as measured by a residual gas analyzer

The desorption data seen in Figure 4 has some interesting features. It is clear that desorption of Ga from GaN is not constant with time - it falls during the high temperature anneal. There may be a self-limiting process occurring. As the GaN thickness decreases, the absorption of black body heat from the heater falls, the surface cools, the bandgap rises and further reduces absorption. During the growth of GaN following the anneal, it can be seen that the Ga desorption varies with time. The same argument can be applied here. As the GaN layer becomes thicker, it absorbs more black body radiation from the hot surfaces below, becomes warmer, its bandgap shrinks and

thereby raises absorption of more of the black body radiation. Eventually, thickness does not play a role in epi-layer temperature when the layer is several absorption lengths thick.

GaN has been grown on 4H SiC obtained from Northrop Grumman. Significant differences in GaN behavior are seen compared to growth of GaN on sapphire substrates. When GaN is grown on SiC, it can be seen t by RHEED that GaN desorbs at substrate thermocouple temperatures in the range of 800°C to 900°C which is similar to other reports of congruent sublimation of GaN. When GaN is grown on sapphire, heating to the thermocouple temperature of 1200°C shows insignificant desorption. The two different substrates produce vastly different surface temperatures for identical backside coating (with tungsten), and mounting (using In-free mounts). Since SiC is less transparent into UV wavelengths, we think that it is a better absorber of blackbody radiation, in addition to having better thermal conductivity at growth temperatures than sapphire. We have begun to model the absorption of blackbody heat by GaN on sapphire as a function of thickness and will seek to understand this behavior.

A better measurement of actual GaN epitaxial layers is needed. We are presently testing high temperature PL measurements of GaN to determine its actual temperature in the MBE chamber. We have proposed a DURIP equipment upgrade to fabricate a combined PL and optical reflectance spectroscopy system to determine the temperature of GaN in-situ.

The optimized growth conditions have been used to grow GaN MESFETs and vertical ballistic transistors for processing at Cornell. The MESFET materials were made from n-GaN doped at $1x10^{19}$ cm^{-3} with 300K mobility of approximately 60 $cm^2/Vsec$. Another MESFET sample had an initial 300K mobility of roughly 300 $cm^2/Vsec$ and a sheet density of $1.3x10^{13}$ cm^{-2} . It is believed that this mobility measurement underestimated the 2-DEG mobility as a result of parasitic conduction in the buffer layer. Efforts are underway to improve on the Schottky barriers formed on these devices so that the material can be more thoroughly studied.

While trying out the new RF source, an unexpected observation was made. It has been found that mobilities of 200 can only be obtained when growing on 2 inch diameter sapphire (with a single exception). We had been using only 1/4 of 2 inch sapphire substrates for economy. For the remaining development of GaN on sapphire, we will now only use full 2 inch substrates. The goal of the program is to move entirely onto SiC, but SiC wafers remain in short supply.

E. Flow Modulation Epitaxy of GaN Buffer Layers - J.A. Smart and J.R. Shealy

1. Progress

The lack of suitable substrates for GaN based material systems have lead researchers into development of nitride based buffer layers on latticed mismatched materials. Starting substrates explored include GaAs, silicon, sapphire, and SiC, with sapphire presently being the most widely used. Accepted techniques for producing GaN buffers on sapphire using conventional OMVPE involves three growth segments. First, the Al_2O_3 surface is converted to AlN by exposure to nitrogen, usually supplied as NH_3. Next, a thin (<1000Å) low temperature (500°C to 600°C) GaN nucleation layer is grown followed by a high temperature GaN buffer layer. The high temperature film is one of the more critical steps as conditions must be found which initially creates large isolated islands which eventually coalesce into a planar surface. In our case we have increased the substrate temperature to roughly 1100 °C in order to enhance the lateral growth rate to achieve

planarization. Structural and transport properties of the top GaN layer are evaluated to optimize the growth parameters involved in the nitridation and nucleation steps.

Initially, a series of runs grown on sapphire were performed with nucleation temperatures varied from 530°C to 670°C. The nucleation layer thickness was targeted for 500Å, while the GaN top layer was held constant at 1μm with a growth temperature of 1030°C. Nitridation of the substrate surface was initially done at 550°C with ammonia exposure for 60 sec. A temperature of 600°C provided the narrowest FWHM X-ray peak (0002 reflection) from the top GaN layer as shown in Figure 1. To further improve structural quality the nitridation temperature was increased to 1030°C, aiding the surface conversion of Al_2O_3 to AlN. A greater than 25% reduction in the X-ray FWHM was measured as presented in Figure 1.

After defining the optimal nucleation growth temperature, the thickness of this layer was varied to determine its effects on coalescence and mobilities of the top GaN layer. In this case a series of runs were done with nucleation layer thicknesses varied from 65Å to 500Å. Best room temperature mobilities of 58 $cm^2volt^{-1}sec^{-1}$ were measured on 1 μm thick layers with 125Å thick nucleation layers. These samples exhibited unintentional electron carrier concentrations of $\approx 10^{20}$ cm^{-3} and pyramid-like growth surfaces. Hexagon pyramids present on the growth surface indicate too low a ratio between lateral to vertical growth rates. To enhance the lateral growth rate within the GaN overlayer, the growth temperature was increased from 1030°C to 1100°C.

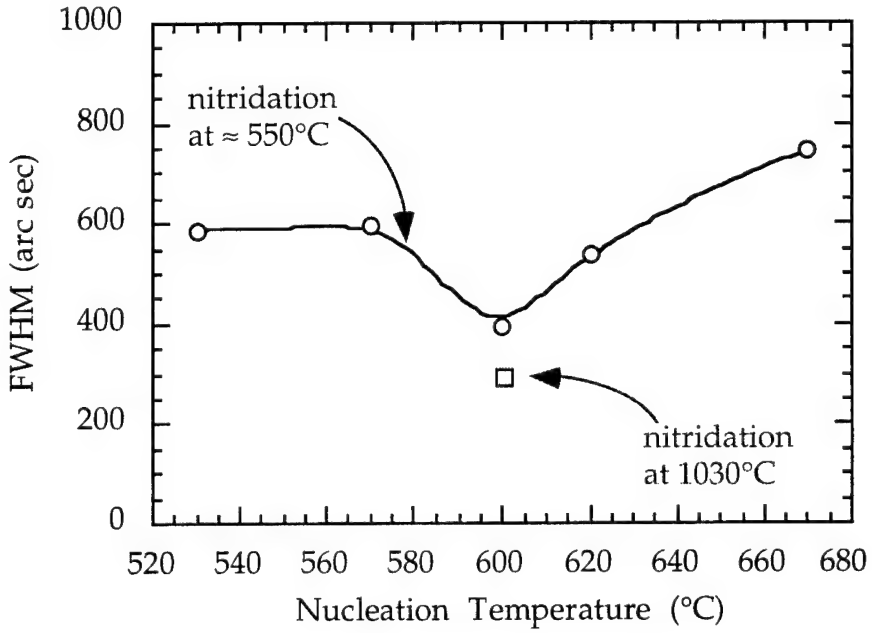


Figure 1. X-ray (0002) diffraction FWHM of GaN buffer layer. Nitridation time held constant at 60 sec while at either 550°C or 1030°C, while nucleation growth temperatures were varied.

Surface morphologies of these layers improved dramatically but pyramid-like structures with flat tops were still visible on thin layers as shown by the SEM image of Figure 2. However, very smooth surfaces are visible indicating that higher substrate temperatures are desirable. Increasing the growth temperature reduced the growth rate from 1μm/hr to 0.25μm/hr, but increasing the

growth pressure is likely to offset this Ga-desorption related growth rate reduction. Layers with nominal thicknesses of 0.25μm yielded mobilities of 130 $cm^2 volt^{-1} sec^{-1}$ with background carrier concentration in the low 10^{18} cm^{-3}.

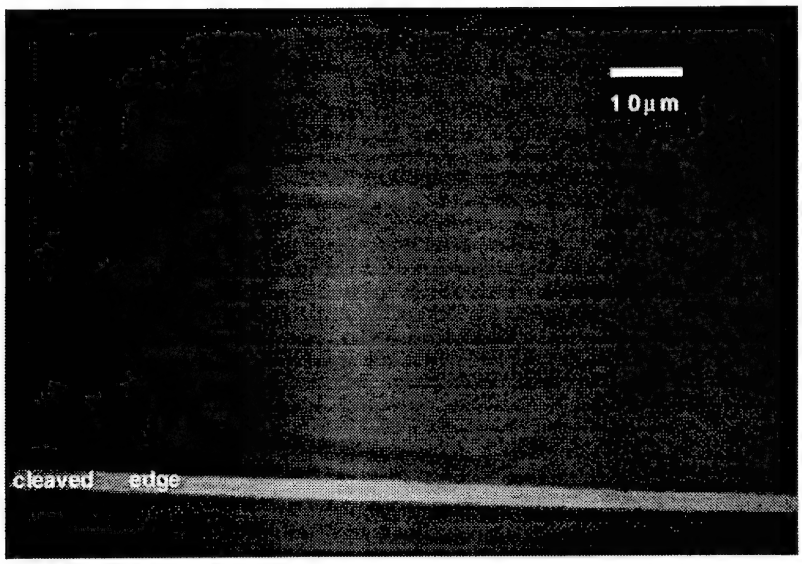


Figure 2. SEM micrograph of "pyramid-like" structures with plateau top at 1100°C growth temperature. GaN overlayer thickness of 0.25 μm.

One of the primary objectives of this program is obtaining GaN-based transistors on SiC substrates, necessitating the need for developing GaN buffer layers on SiC. Initial results depositing GaN on conducting SiC substrates are promising. Figure 3 shows I-V characteristics of a silicon doped GaN layer on SiC. GaN contacts are Ti/Al with Ti/Pt/Au on the n+ SiC substrate. The SiC contact is ohmic as deposited, with conduction through the buffer showing some rectifying characteristics. Post metallization annealing up to 650°C improves the I-V performance, while higher temperature annealing has negligible effects. Presently we have achieved voltage drops as low as 1 volts at 100 amps/cm^2 through this heterointerface.

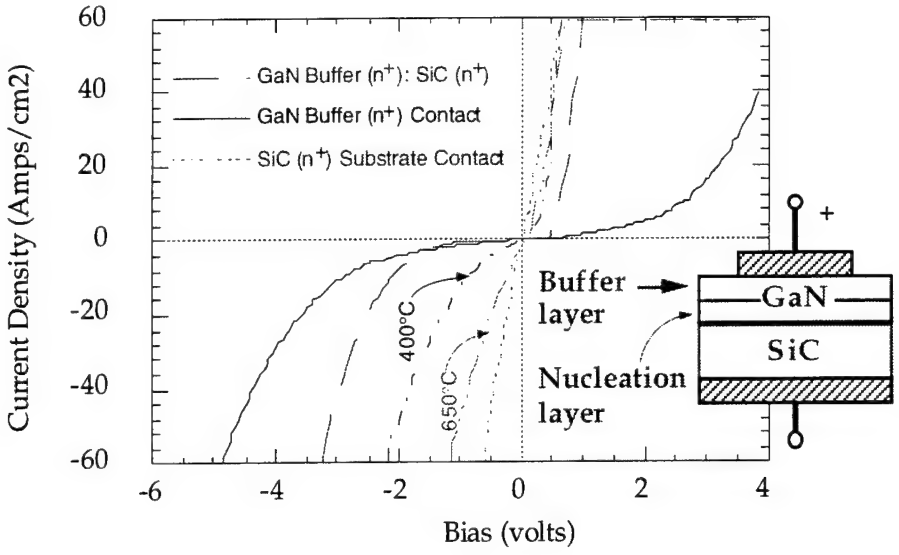


Figure 3. GaN:Si buffer layer grown on cubic SiC. Si doped GaN layer is 1 μm thick, doped to low 10^{18} cm^{-3}.

2. Future studies

Advances have been made in the development of GaN buffer layers on sapphire and SiC substrates using flow modulation OMVPE. Although sapphire substrates are not used directly for the device work in this program, they are used to optimize the best buffer conditions which will be applied to SiC buffer structures. We will investigate thicker GaN films on 6H and 4H semi-insulating SiC to optimize the buffer structures as measured by electron mobility. With acceptable mobilities, lateral conduction device structures will be investigated and provided to other program members. The conducting buffer structures on n-type SiC substrates will be optimized for vertical conduction devices.

F. High Resolution GaN Structures Using UHV STEM - T. Eustis, Prof. J. Silcox

1. Sample Preparation

Sample preparation development of GaN samples grown by MBE at Cornell has begun. Two initial techniques are being attempted. The first is a standard wedge sample where several pieces of a sample to be investigated are bonded together. The specimen is then thinned and polished until a wedge suitable for the mounting and examination is obtained. Figure 1 portrays a typical sample with typical dimensions.

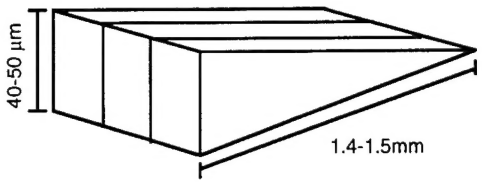


Figure 1

The tip of the wedge is polished to be less than 1 µm thick and possibly thin enough for examination in the STEM. However if the tip is too thick for examination, the sample is thinned further by ion milling.

Initial sample preparation involved sandwiching together four slices of GaN sample with a silicon center wafer for a total of five layers. Four slices of the GaN sample were used in an attempt to increase the probability of obtaining a useful sample. The silicon wafer, being the only opaque material, allows for location of the specimen when mounted on the glass sample mount and when in solvents. In addition, silicon undergoes a color change when thinned and thus provides an estimate of the thickness of the sample. Finally, when examining the specimen in the STEM, silicon allows for easy calibration of the STEM, easy orientation of the sample, and an accurate determination of the magnification.

A second specimen preparation technique suitable only for interface investigation was attempted. The possible advantage of this technique is speed, as a sample can be prepared and investigated in a single day. First, most of the substrate is polished off of a sample, which is roughly $1mm^2$. The sample is then fractured into a powder. The powder is placed on a carbon grid sample mount and examined. With the tens of thousands of sample fragments, the hope was that the probability of finding a useful fragment would be high. However, from initial attempts this technique is inhibited in two ways. First, the GaN and sapphire appear to fracture easily from each other preventing examination of the interface. Secondly, the GaN seems to fracture into balls instead of the desired shard shape. Thus the GaN fragments are not thin enough for examination.

2. Current Work

Two key tools being used in the current investigation are the high resolution images obtainable from the STEM and Parallel Electron Energy Loss Spectroscopy (PEELS) available in the STEM. PEELS provides a rapid and convenient measure of local composition. It also probes the unoccupied states in the gap and in the conduction band. Atomic scale resolution of the local density of states can be obtained.

Figure 1 is an image of the thin tip of a sample wedge. The different areas are labeled.

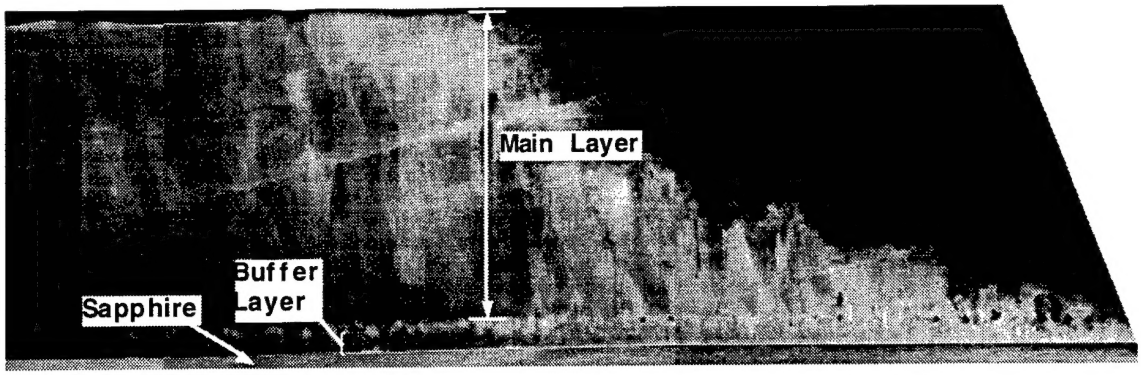
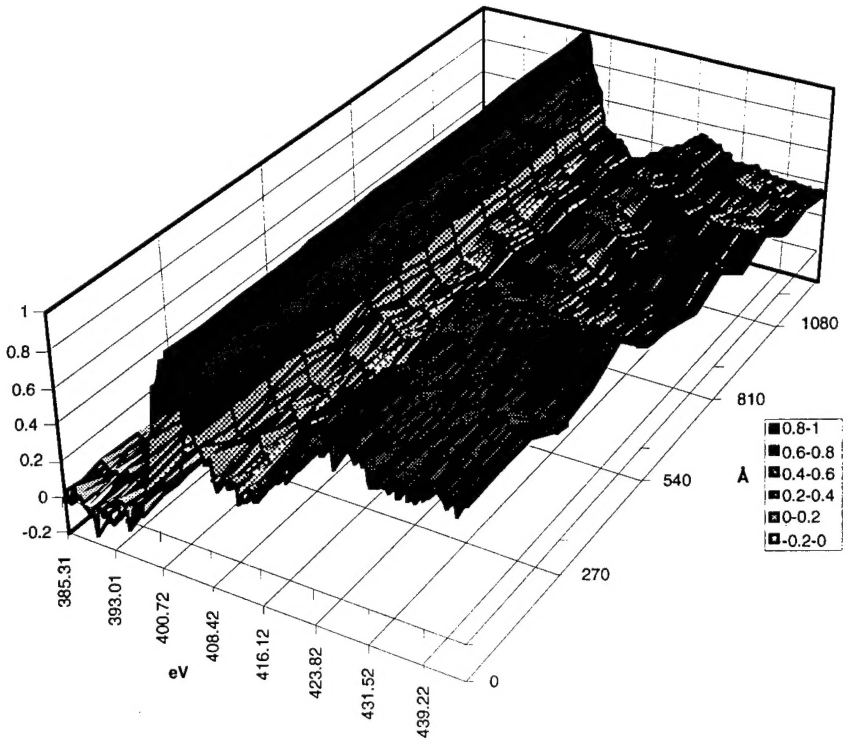


Figure 1

There appears to be something at the interface between the buffer layer and the main layer. The dark and light dots were examined with PEELS. The PEELS revealed the dark spots were no different in composition or bonding than the material around them. However the light spots are located in areas which are too thick for examination with PEELS. Thus it is believed that whatever was at the interface where the black spots are has either fallen out or been exposed and etched out during a final preparation step. X-ray analysis of the light spots will be performed in an attempt to identify them.

PEELS was also employed to examine any difference in bonding between the buffer layer and the main layer. A series of spectra of the nitrogen K-edge was taken going across the buffer / main layer interface. The zero Å point corresponds to a point in the main layer and the 1260 Å point corresponds to a point in the buffer layer. The interface is at about 600Å. The spectra are displayed in Graph 1



Graph 1

After scaling for thickness, the only difference in the spectra can be seen is in the peak occurring around 423 eV. The change in the intensity of the 423 eV peak is caused by increased interaction of the electrons with plasmons due to thickness. Thus there is not a noticeable difference in the local density of state and thus the bonding between the buffer layer and the main layer.

3. Future Work

Two future avenues of investigation have been initiated. The first is a continuing investigation of the buffer layers grown at Cornell by MBE. As seen above, this work has already begun. The second is a look into the notorious "yellow band" (YB) found in PL measurements.

The buffer layer seems to be key in obtaining quality material. In addition, it appears that the buffer layer is the key difference between the quality obtained by MBE and MOCVD. Several advances at Cornell have been made in the MBE grown buffer layers. These advances as well as continuing advances will be examined in an attempt to understand the characteristics that lead to quality films

It has been debated whether the nitridization of the sapphire substrate by the nitrogen plasma sources used by MBE converts the surface of the sapphire to AlN providing a better surface for GaN nucleation and growth. PEELS will permit us to determine if the surface is a nitride, an oxide, or an oxynitride as each have a specific "fingerprint" spectrum. Lattice imaging of the buffer layer will permit us to determine the microstructure that leads to the highest quality material.

The YB is a topic of intense debate in the GaN community. At Cornell, it is believed the odd trends in mobility might be related to the YB defects. The location of the energy level(s) responsible for the YB can be determined with PEELS. If the YB is 2.2 eV from the conduction

band a peak 2.2 eV from the onset of the nitrogen K-edge will be observed. If the YB is 2.2 eV from the valence band a peak 2.2 eV after the zero-loss peak well be observed. Samples can be easily mapped using the observed defect PEELS peak to determine with atomic resolution what areas and thus what microstructure is producing the YB. In general, it is believed that the YB is caused by point defects. The two point defects given the greatest probability of causing the YB are the gallium vacancy and the nitrogen vacancy. However, evenly distributed point defects can not explain the width of the YB nor the variation in YB intensity with doping. Local high concentrations of point defects could explain both of these observations. Such local high concentrations could be located at or near dislocations. It is well known that dislocations produce strain fields creating energetically favorable gettering regions. High concentrations of point defects can be detected by PEELS. The states associated with nitrogen are easiest to resolve and the most influenced by changes in the local atomic structure. Gallium vacancies or nitrogen vacancies changing the local atomic structure as the lattice relaxes will produce distinguishable changes in the nitrogen K-edge permitting determination of the defect.